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RESEARCH ARTICLE

Analysis of time software and hardware delays in audio module circuits with cyber-physical SPICE emulation

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Abstract

Objectives. The study sets out to parametrically investigate the impact of time delays within cyber-physical emulation circuits for signal audio modules. Specifically, it examines how delays introduced by analog-to-digital and digital-to-analog converters of the hardware/software interface, the central processor, and the visual graphical emulation (VGE) software environment are influenced by factors like the selected data input-output protocol and the VGE block preset configurations such as sampling rate, buffer size and time, and the number of channels.

Methods. Used methods of architectural SPICE[1] modeling of electrical circuits on the VGE *Simulink* software platforms leverage the resources of the Simscape library and *LiveSPICE*. Additional methods include those for incorporating differential equations in the numerical analysis of SPICE models designed for analog circuits and techniques for processing experimental data generated from cyber-physical emulation using the built-in *Simulink* environment and associated laboratory radio measurement tools.

Results. The study introduces a novel approach to emulate analog audio devices using cyber-physical SPICE modeling. Through the use of digital twins, the study investigates the impact of modifiable parameters on signal delays within audio module circuits during cyber-physical emulation. Based on these findings, technical guidelines are provided for selecting appropriate delay correction settings between 20 and 120 ms to ensure efficient high-speed audio signal post-processing.

Conclusions. By configuring the VGE software block's settings identically to the ASIO[2] data input/output protocol prevalent in audio interface technology (44.1 kHz sampling frequency, 8 buffer size) substantially decreased latency in typical audio module circuit nodes is achieved with cyber-physical emulation built into the VGE *LiveSPICE* environment. The achieved time delays of 5 ms direct transmission circuit contrast with the 7 ms latency observed in the cyber-physical emulation of the SPICE circuit when both are benchmarked within the VGE *Simulink* environment. The

[1] SPICE (Simulation Program with Integrated Circuit Emphasis) is an open-source simulator for general-purpose electronic circuits.

[2] Audio Stream Input/Output is a low-latency data transmission technology providing applications with a uniform interface to hardware resources.

successful implementation of cyber-physical emulation for SPICE models is achieved through the use of particular settings, such as a 44.1 kHz sampling frequency, buffer sizes ranging from 512 to 1024 samples, and the use of the ASIO data input/output protocol.

Keywords: time delay, correction, cyber-physical SPICE emulation, Simulink, LiveSPICE, Simscape, audio interface, ASIO, signal audio module

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НАУЧНАЯ СТАТЬЯ

Анализ временных программно-аппаратных задержек в схемах аудиомодулей с киберфизической SPICE-эмуляцией

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Резюме

Цели. Цель статьи – параметрический анализ влияния временных задержек в схемах киберфизической эмуляции сигнальных аудиомодулей, вносимых аналого-цифровыми и цифро-аналоговыми преобразователями программно-аппаратного интерфейса, центральным процессором и программной средой визуально-графической эмуляции (ВГЭ) в зависимости от выбранного протокола «ввода-вывода» данных и установленных преднастроек программного блока ВГЭ, таких как частота дискретизации, размер и время буфера, число каналов.

Методы. Применяются методы архитектурного SPICE[3]-моделирования электрических схем на программных платформах ВГЭ *Simulink*, в т.ч. с использованием ресурсов библиотеки Simscape, и *LiveSPICE*; методы интегрирования дифференциальных уравнений при численном анализе SPICE-моделей аналоговых схем; методы обработки экспериментальных данных киберфизической эмуляции с помощью встроенных средств среды *Simulink* и лабораторного радиоизмерительного оборудования.

Результаты. Предложен метод киберфизической SPICE-эмуляции аналоговых аудиоустройств. Получены результаты анализа формирования временных задержек в схемах сигнальных аудиомодулей с киберфизической эмуляцией при вариации преднастраиваемых параметров, влияющих на задержки сигналов, с применением двойников. Разработаны технические рекомендации выбора корректирующих параметров временных задержек от 20 до 120 мс для обеспечения постобработки аудиосигнала.

Выводы. Показано, что для часто используемого в аудиоинтерфейсной технике протокола «ввода-вывода» данных ASIO[4] при тождественно установленных преднастройках программного блока ВГЭ (частота

[3] SPICE (англ. Simulation Program with Integrated Circuit Emphasis) – программа-симулятор электронных схем общего назначения с открытым исходным кодом. [SPICE (Simulation Program with Integrated Circuit Emphasis) is an open source simulator of general-purpose electronic circuits.]

[4] Audio Stream Input/Output, «ввод-вывод потоковых аудиоданных» – протокол передачи данных с малой задержкой, предоставляющий приложениям унифицированный интерфейс к аппаратным ресурсам. [Audio Stream Input/Output is a low-latency data transmission technology providing applications with a uniform interface to hardware resources.]

дискретизации 44.1 кГц, размер буфера 8) типовые функциональные узлы схем аудиомодулей с киберфизической эмуляцией, построенные в среде ВГЭ *LiveSPICE*, имеют наименьшие временные задержки 5 мс – для схемы прямого прохождения сигнала и 7 мс – в случае с киберфизической эмуляцией SPICE-схемы в отношении к их реализации в среде ВГЭ *Simulink*. Установлено, что обоснованно выбранными настройками при практической реализации метода киберфизической эмуляции SPICE-моделей являются: частота дискретизации 44.1 кГц, размер буфера от 512 до 1024 семплов и протокол «ввода-вывода» данных ASIO.

Ключевые слова: временные задержки, киберфизическая SPICE-эмуляция, Simulink, LiveSPICE, Simscape, аудиоинтерфейс, ASIO, сигнальный аудиомодуль

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INTRODUCTION

A widely recognized classification for digital representations of electrical circuits used in automated circuit design and software-based numerical analysis of functional units within radio-electronic equipment includes code-based, visual-graphical, and hybrid approaches [1]. For example, the use of program code to interpret the hardware architecture of functional circuits in signal radio modules necessitates the utilization of specialized languages like SPICE[5], VHDL[6], or object-oriented programming languages such as C/C++, Java, Python, Ruby, etc. Visual-graphical descriptions offer code-based interpretations of circuit and functional architectures by employing functional blocks connected in a directed graph. Mixed emulation involves a variable combination of code, block, and specialized hardware description languages to represent circuit elements along with their corresponding electrical and logical interconnections.

The SPICE emulator [2], representing a typical means of interpreting analog circuit solutions, is based on numerical methods for integrating differential systems of equations in order to determine the currents and voltages in a given electrical circuit.

Electronic component base (ECB) manufacturers, including Texas Instruments[7], Linear Technology[8], KYOCERA AVX[9], STMicroelectronics[10] and others, offer design engineers access to parametric SPICE models and vector S-parameter models for ECB libraries, which are all backed by experimentally validated performance data. By leveraging original ECB libraries with comprehensive parameterization tailored to specific equivalent models, which are constructed upon a popular SPICE emulator platform, an electronic printed circuit board's radio-technical attributes can be closely aligned with the outcomes of its circuit emulation within a condensed timeframe.

Examples of visual-graphical design tools include *SigmaStudio*[11], *LTSPICE*[12], *QSPICE*[13], *Tina-TI*[14], and *NI Multisim*[15]. These automated visual design platforms, which operate with hidden code, facilitate the creation of electronic product circuit architectures of any configuration by utilizing library blocks and modules. However, a drawback of these automated platforms is their inability to enable real-time modifications to block descriptions through user-defined program code. Platforms like *LabView*[16], *Simulink*, *Proteus Design Suite*[17], and some others circumvent this limitation with visual graphical emulation (VGE). VGE platforms, which may be categorized as mixed description, allow

[5] SPICE (Simulation Program with Integrated Circuit Emphasis) is an open source simulator for general-purpose electronic circuits.

[6] VHDL is a Very High Speed Integrated Circuit (VHSIC) Hardware Description Language.

[7] Texas Instruments official website. https://www.ti.com/. Accessed February 20, 2025.

[8] https://lineartech.com/. Accessed February 20, 2025.

[9] https://www.kyocera-avx.com/. Accessed February 20, 2025.

[10] https://www.st.com/. Accessed February 20, 2025.

[11] https://wiki.analog.com/resources/tools-software/sigmastudio. Accessed February 20, 2025.

[12] https://www.quadcept.com/en/service/simulation/ltspice/. Accessed February 20, 2025.

[13] https://www.qorvo.com/design-hub/design-tools/interactive/qspice. Accessed February 20, 2025.

[14] https://designsoftware.com/home/English/. Accessed February 20, 2025.

[15] https://www.ni.com/en/support/downloads/software-products/download.multisim.html?srsltid=AfmBOopwVYxFcVbXG5r0bM3lm203f24w4RwAIITsF3NAp9On-4a8eb_F#452133. Accessed February 20, 2025.

[16] https://www.ni.com/en/shop/labview.html?srsltid=AfmBOoowwWPAjm-J6TthCp-LDLqR2ikpuO0W5eJHBp2ukB0E3Xe00cfO. Accessed February 20, 2025.

[17] https://proteus.no/proteus.html. Accessed February 20, 2025.

modifications to blocks through code written in high-level or command-based programming languages.

The VGE *LiveSPICE*[18] environment, a cyber-physical platform developed by inventor Dillon Sharlet, provides a unique solution for emulating audio modules using SPICE. This software environment empowers users to design, analyze, and debug electrical audio circuits built on the ASIO[19] protocol. It facilitates this process by enabling real-time signal transmission between the audio interface and the SPICE model of the circuit.

Sharlet's cyber-physical SPICE emulation technique, which was initially applied within the VGE *LiveSPICE* platform, holds significant value for various research endeavors. By integrating physically authentic signals from external circuit-hardware solutions in real-time mode, its implementation can empower the development, debugging, and examination of analog low-frequency SPICE circuits. Nevertheless, implementing this method in an engineering setting necessitates a shift towards multifunctional VGE platforms that incorporate diverse circuit descriptions and a broader library selection. Furthermore, open access to user-friendly software, like *Simulink*, is crucial for this adaptation.

This technique substitutes the hardware module or functional component within a real radio-electronic device's circuit design with a cyber-circuit constructed using the VGE software platform, which is designed for signal analysis and debugging.

1. ANALYSIS OF THE IMPACT OF TEMPORARY DELAYS IN AUDIO SIGNAL DEVICE CIRCUITS WITH CYBER-PHYSICAL EMULATION

The functional circuit of the cyber-physical SPICE emulation method (Fig. 1) demonstrates signal transmission via the input-output (I/O) protocol connecting the software/hardware interface (audio interface) with the pre-installed VGE environment. The audio signal is directed to the input channels of the analog-to-digital converter (ADC) within the software/hardware interface. This interface, which communicates with a computer using a USB connection, sends signal data to the VGE system via the audio signal transmission protocol facilitated by a driver. The VGE system manipulates the signal and sends the modified signal back to the interface, which subsequently directs it to a digital-to-analog converter (DAC) through designated output channels.

Beyond ADC/DAC performance and I/O protocol latencies, several key VGE software block parameters influence the time delays encountered as an input signal traverses the software/hardware interface, driver, and VGE system. These parameters include sampling frequency, buffer size and duration, the quantity of hardware channels utilized, and others. The total accumulated time delay, denoted as $T_{\text{TD accum}}$, can be expressed using the following general formula:

$$T_{\text{TD accum}} = T_{\text{HTD}} + T_{\text{TD VGE}}, \quad (1)$$

where T_{HTD} is hardware time delays and $T_{\text{TD VGE}}$ is time delays introduced by the VGE block.

The hardware time delays during audio interface processing, T_{INTF}, are described by the following equation:

$$T_{\text{INTF}} = T_{\text{DAC}} + T_{\text{ADC}} + T_{\text{Buff.}} + T_{\text{Res.}} + T_{\text{SR}}, \quad (2)$$

where T_{DAC} is the time delays introduced by DAC output channels of the software/hardware interface; T_{ADC} is the time delays introduced by ADC input channels of the software/hardware interface; $T_{\text{Buff.}}$ is the time delays introduced by the buffer of the software/hardware interface; $T_{\text{Res.}}$ is the time delays defined by the ADC/DAC resolution of the software/hardware interface I/O channel; T_{SF} is time delays defined by the sampling frequency.

Audio equipment exhibits a noticeable time lag when the delay exceeds 20 ms; delays shorter than this threshold are generally inaudible. Within circuit analysis, delays up to 130 ms[20] are considered acceptable.

Within the VGE *Simulink* platform, a plugin is developed to simulate signal audio modules in a cyber-physical context by analyzing time delays within these emulated circuits. The replacement of actual audio module with the digital SPICE twin facilitates real-time development and debugging of audio modules using the *Simulink*'s Simscape library. This approach is further utilized to investigate key characteristics mentioned in the introduction, such as buffer size and sampling frequency[21] [3, 4]. The functional circuit of the plugin is shown in Fig. 2.

[18] The *LiveSPICE* developer official website. https://www.livespice.org/. Accessed February 20, 2025.

[19] Audio Stream Input/Output is a low-latency data transmission technology providing applications with a uniform interface to hardware resources.

[20] What is the latency in audio recording? https://taplic.com/audio-tips/latency-in-audio/. Accessed February 20, 2025.

[21] Levchenko N.R., Kostin M.S., Filatov S.V., Pechenkin S.M. *Audio Interface Switching Program with SPICE Technology*: Certificate of State Registration of Computer Program 2024685518 RF. Publ. 30.10.2024 (in Russ.).

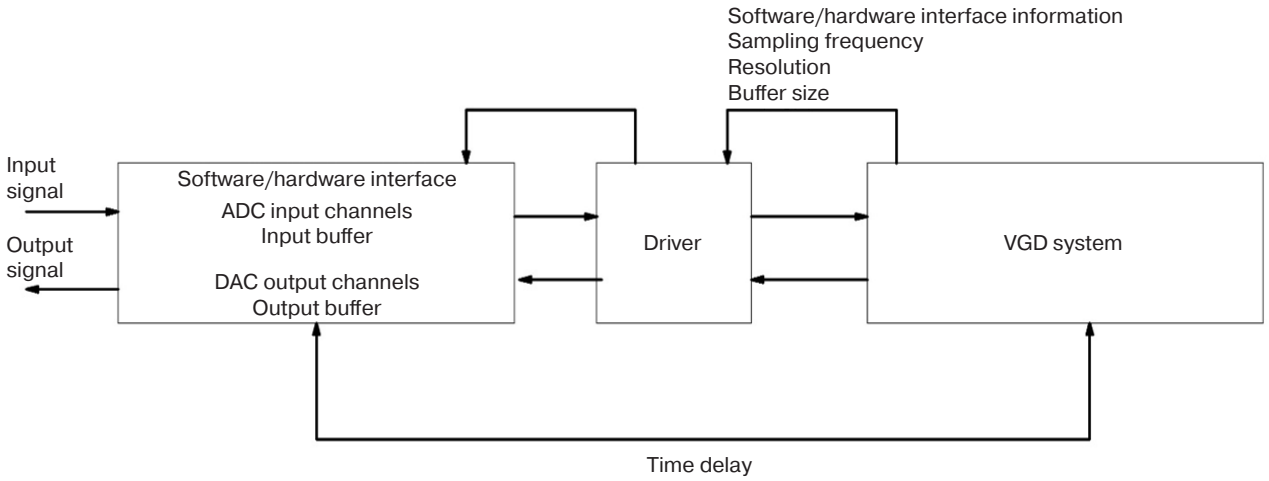

Fig. 1. Functional circuit for implementing the cyber-physical SPICE emulation method. The VGE system is a visual graphic design system

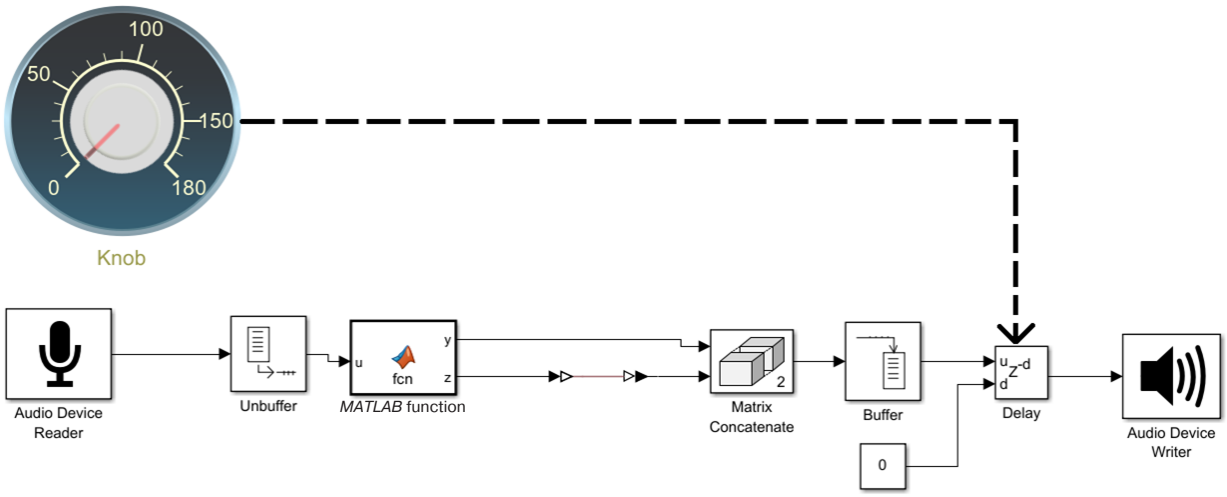

Fig. 2. Functional circuit of the plugin for cyber-physical emulation of signal audio modules in the VGE *Simulink* environment

This plugin comprises the following functional blocks:

1. "Audio Device Reader" block designed to initialize input channels for a software or hardware interface using a defined protocol.
2. "Unbuffer" block for transforming incoming frames from the software/hardware interface into a continuous stream of samples.
3. "*MATLAB* function" serving as a crucial block-level function, serving to isolate the channels within the software/hardware interface.
4. "Matrix Concatenate" block used to construct an $M \times N$ matrix, with M representing the number of samples and N denoting the quantity of channels utilized.
5. "Buffer" block used to convert the resulting matrix into frames, enabling subsequent transmission to the software or hardware interface.
6. "Delay" block used to counteract phase shift before the signal is sent to the software/hardware interface output channels.
7. "Audio Device Writer" block used for capturing incoming audio frames and sending them to the designated output channels of the software/hardware interface.
8. "Knob" block representing a digital potentiometer for adjusting the phase shift within the "Delay" block.

2. EXPERIMENTAL STUDY OF TIME DELAYS IN AUDIO MODULE CIRCUITS WITH CYBER-PHYSICAL SPICE EMULATION

The study evaluates the impact of hardware/software interface elements, including buffer size, resolution, sampling frequency, and audio data transmission

protocol, on the time delays experienced during signal transmission. Two distinct VGE platforms are evaluated: *LiveSPICE* and *Simulink*, together with its specialized plugin for cyber-physical SPICE emulation of signal audio modules. The selected software/hardware interface for this study is the UMC1820 audio interface (Behringer, Germany). Users have the flexibility to select from various parameters, including buffer size options ranging from 8 to 2048 samples, sampling frequencies at 44.1, 48.0, 88.2, and 96.0 kHz, and support for data transfer protocols like ASIO, WASAPI[22], and DirectSound [5–7].

The scheme of cyber-physical emulation of signal audio modules is shown in Fig. 3.

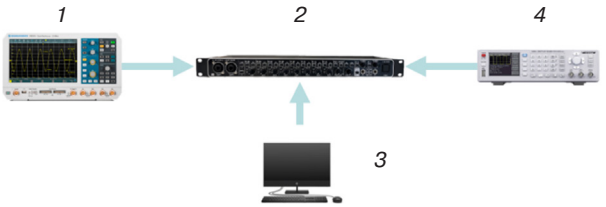

Fig. 3. Scheme of cyber-physical emulation used to explore time delays: *1* is oscilloscope RTB2002 (Rohde & Schwarz, Germany); *2* is audio interface UMC1820; *3* is personal computer; *4* is signal generator HMF2550 (Rohde & Schwarz, Germany)

The time delays τ_{DLY} obtained from a cyber-physical emulation setup are presented in Table 1. This setup employs varying sampling frequencies F_S while maintaining a constant buffer size of N = 2048 for a straightforward, single-channel audio stream directly from input to output of the audio interface.

Table 1. Outcomes of examining time delays that occur when adjusting sampling frequency while maintaining a constant buffer size

VGE environment, data I/O protocol							
LiveSPICE, ASIO		*Simulink*, ASIO		*Simulink*, DirectSound		*Simulink*, WASAPI	
F_S, kHz	τ_{DLY}, ms	F_S, kHz	τ_{DLY}, ms	F_S, kHz	τ_{DLY}, ms	F_S, kHz	τ_{DLY}, ms
44.1	81.8	44.1	128	44.1	174	44.1	135
48	78.6	48	121	48	162	48	130
88.2	71	88.2	104	88.2	110	88.2	108
96	70	96	98.8	96	108	96	100

The findings from research on the VGE *LiveSPICE* environment utilizing DirectSound and WASAPI protocols remain unpublished because the VGE *LiveSPICE* environment is inherently designed to operate exclusively with the ASIO protocol.

The time delays incurred by varying the buffer size N are presented in Table 2. These measurements are taken with a constant sampling frequency F_S = 44.1 kHz via a single-channel direct streaming method between the audio interface's input and output, which utilizes the ASIO, DirectSound, and WASAPI protocols.

Table 2. Outcomes of examining time delays that occur when adjusting the buffer size while maintaining a constant sampling frequency

VGE environment, data I/O protocol							
LiveSPICE, ASIO		*Simulink*, ASIO		*Simulink*, DirectSound		*Simulink*, WASAPI	
N	τ_{DLY}, ms	*N*	τ_{DLY}, ms	*N*	τ_{DLY}, ms	*N*	τ_{DLY}, ms
8	5	8	81.8	8	–	8	90
16	5	16	82.4	16	–	16	92
32	6	32	82.4	32	–	32	92
64	6.6	64	82.4	64	–	64	92
128	8.6	128	85.4	128	–	128	95
256	13.8	256	88.4	256	103	256	99
512	23.2	512	93.8	512	109	512	100
1024	42.8	1024	105.8	1024	111	1024	107
2048	82	2048	129	2048	164	2048	135

It can be seen from Tables 1 and 2 that adjusting the buffer size in the software/hardware interface for both the direct signal transmission method and the DirectSound audio protocol leads to longer transmission delays. Notably, the *Simulink* environment's direct signal pathway, when coupled with the cyber-physical emulation plugin and DirectSound transmission, exhibits the most significant delay, reaching 174 ms. Direct signal transmission within the *LiveSPICE* platform demonstrated very short delays down to 5 ms. Interestingly, buffer overflow leads to reduced time delays when the sampling frequency is elevated [8–10].

For assessing time delays within VGE systems using a digital SPICE twin, a standard low-frequency amplifier (LFA) circuit is utilized. The LFA fundamental circuit designs, which were developed on VGE *Simulink* platforms leveraging the Simscape library and *LiveSPICE*, are shown in Figs. 4 and 5. The use of a standard LFA circuit for analyzing and adjusting time delay properties in analog circuits with cyber-physical SPICE simulation is justified by the common circuit solutions of audio mixer consoles (such as active equalization lines, preamps, summers, panoramic dividers, and others) based on operational amplifiers (OAs) [11–13].

[22] Windows Audio Session API is a low-latency data transfer protocol providing applications with a unified interface to hardware resources, developed by Microsoft.

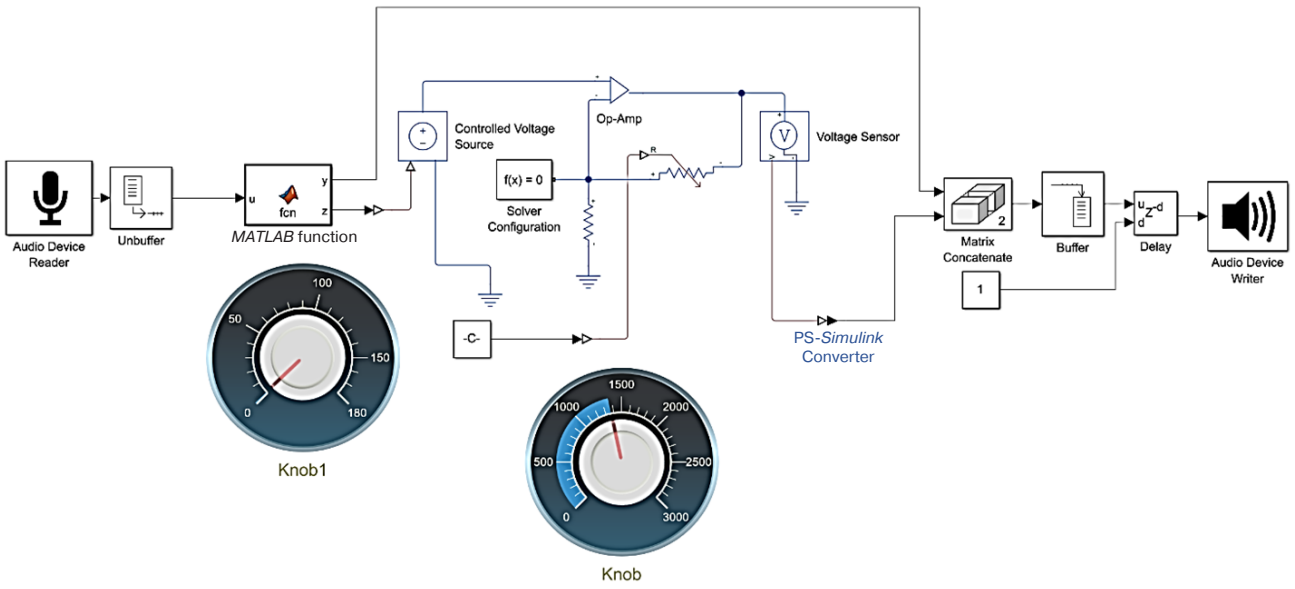

Fig. 4. LFA circuit in the VGE *Simulink* environment for analyzing time delays

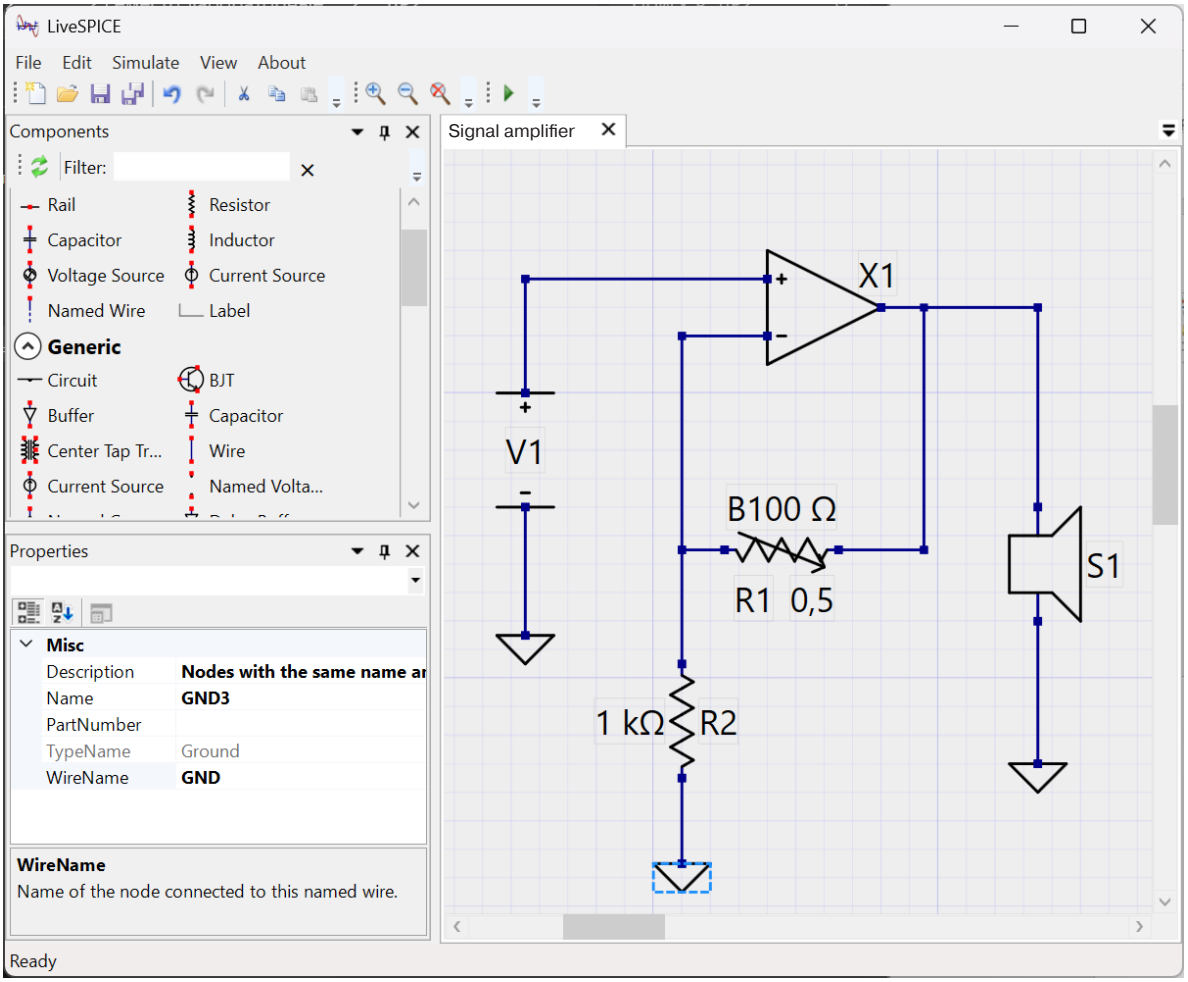

Fig. 5. LFA model circuit in the VGE *LiveSPICE* environment for analyzing time delays.
The designations of the circuit elements correspond to those adopted in GOST 2.710-811[23]

[23] GOST 2.710-81. Interstate Standard. *Unified system for design documentation. Alpha-numerical designations in electrical diagrams*. Moscow: Izd. Standartov; 1985 (in Russ.).

The time delays resulting from varying the sampling frequency, F_S, within a digital twin of the power amplifier audio module are presented in Table 3, with a constant buffer size of $N = 2048$.

Table 3. Outcomes of examining time delays in a power amplifier's audio module by simulating various sampling frequencies within a digital twin model while maintaining a constant buffer size

VGE environment, data I/O protocol							
LiveSPICE, ASIO		*Simulink*, ASIO		*Simulink*, DirectSound		*Simulink*, WASAPI	
F_S, kHz	τ_{DLY}, ms	F_S, kHz	τ_{DLY}, ms	F_S, kHz	τ_{DLY}, ms	F_S, kHz	τ_{DLY}, ms
44.1	100	44.1	194	44.1	398	44.1	220
48	96	48	182	48	384	48	205
88.2	95	88.2	146	88.2	362	88.2	182
96	95	96	137	96	351	96	157

The time delays resulting from varying buffer size N within the LFA audio module using a digital twin model and maintaining a constant sampling frequency of $F_S = 44.1$ kHz are given in Table 4.

Table 4. The outcomes of examining time delays in a power amplifier's audio module by simulating various buffer sizes while maintaining a constant sampling frequency

VGE environment, data I/O protocol							
LiveSPICE, ASIO		*Simulink*, ASIO		*Simulink*, DirectSound		*Simulink*, WASAPI	
N	τ_{DLY}, ms	N	τ_{DLY}, ms	N	τ_{DLY}, ms	N	τ_{DLY}, ms
8	7	8	100	8	–	8	110
16	7.2	16	100.4	16	–	16	110.2
32	7.4	32	101.2	32	–	32	111.5
64	8	64	102.8	64	–	64	113.3
128	11.6	128	105.2	128	–	128	116.5
256	17.8	256	111.2	256	262	256	118.6
512	29.4	512	124	512	297	512	130
1024	53.2	1024	147	1024	310	1024	150
2048	100	2048	194	2048	398	2048	210

The inclusion of the SPICE circuit results in a doubling of the time delays in comparison to those observed in a direct pass circuit of an operational amplifier without a SPICE model. This increase is attributed to the additional processing time required by the VGE environment software block required to handle the SPICE circuit [10, 14, 15]. Notably, the VGE *LiveSPICE* system exhibits the shortest delay due to the built-in algorithm for calculating the differential equations of the SPICE model just once. Although SPICE integrated algorithm simplifies integral-differential calculations for circuits, its fixed nature hinders its flexibility and restricts the use of pre-built SPICE component libraries from manufacturers as contrasted with the broader capabilities of the Simscape library. Therefore, the formula (2) for hardware delays is presented as follows:

$$T_{INTF} = T_{DAC} + T_{ADC} + T_{Buff.} + T_{Res.} + T_{SR} - T_{VGE}, \quad (3)$$

where T_{VGE} is the time delay introduced by the VGE environment block.

Due to the absence of built-in time measurement tools within the VGE *LiveSPICE* platform, further investigation is conducted in the VGE *Simulink* environment. This research utilizes a custom-developed cyber-physical emulation plugin designed to interact with the Simscape library. Given the ASIO protocol's minimal latency and its widespread use in audio technology [16–18], subsequent research focuses solely on this protocol.

3. MEASURING TIME DELAYS INTRODUCED BY THE SPICE EMULATION BLOCK WITHIN THE *SIMULINK* ENVIRONMENT

For assessing the time delays introduced by the SPICE emulation block in the VGE environment, the built-in *Simulink Profiler*[24] is employed. This tool initiates the simulation and generates a report that may be used to analyze the time delays introduced by the VGE block, which serves as the foundation for the audio module circuit. The window for this tool is shown in Fig. 6.

The time delays introduced by the SPICE emulation block can be evaluated using the obtained parameters as follows:

$$T_{VGE} = \frac{\text{Self Time}}{\text{Number of calls}}, \quad (4)$$

where Self Time is the *Simulink* model operating time, including time for generating the *Simulink Profiler* report,

[24] Technical documentation of *Simulink Profiler*. https://www.mathworks.com/help/simulink/slref/simulinkprofiler.html. Accessed February 20, 2025.

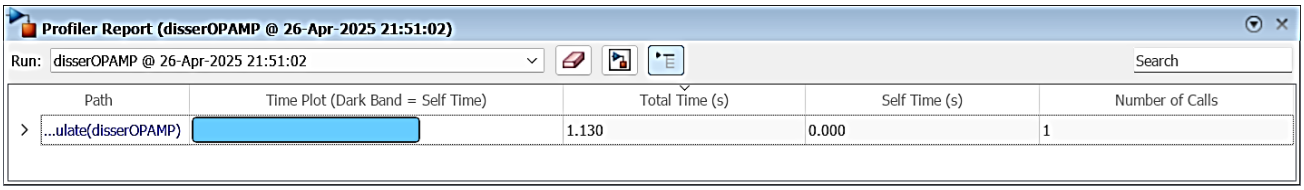

Fig. 6. Window of the built-in *Simulink Profiler* tool with the plugin for cyber-physical emulation of signal audio modules

while Number of Calls is the number of model calls made during Self Time [19, 20].

Tables 5 and 6 present the results of analyzing the time delays introduced by SPICE simulations conducted within *Simulink* for both a direct signal transmission circuit and a circuit utilizing an OA-based LFA.

Table 5. The outcomes of examining the time delays introduced by the SPICE simulation within *Simulink* for the direct signal transmission circuit

Simulink Profiler runtime, s	SPICE simulation time for VGE, ms	SPICE emulation time for VGE with electrical schematic simulation, ms
1	1.2	1.8
2	1.2	1.8
3	1.2	1.8
4	1.2	1.8
5	1.3	1.95

The results presented in Table 5 show that the time delays introduced by the emulation block, taking into account the cyber-physical SPICE emulation of the signal audio module, experience a 1.5-fold augmentation.

Since the VGE *Simulink* environment lacks tools for assessing CPU cycle consumption, a thorough examination of efficiency is impossible. The reported research employed a 64-bit Intel® Core™ i5-10500T (Intel, USA) processor functioning at a frequency of 2.3 GHz.

CONCLUSIONS

The paper presents a novel approach for emulating analog audio systems within a cyber-physical SPICE environment. It proposes an "interface circuit" that utilizes the UMC1820 software/hardware audio interface. The study delves into the time delays inherent in the software/hardware interface of VGE hardware and software systems. Results indicate that the VGE *LiveSPICE* system exhibits the lowest latency (7 ms). This can be attributed to its unique algorithm that calculates SPICE model differential equations only once. Nevertheless, this method lacks flexibility and is incompatible with the utilization of existing SPICE libraries.

Conversely, the VGE *Simulink* system, when enhanced with a plugin for emulating cyber-physical circuits, enables the incorporation of code description of completed PCB models, albeit at the cost of extended time delays (exceeding 100 ms). The *Simulink Profiler* tool is employed to evaluate the computational time delays within the VGE system.

For optimal performance when using the cyber-physical emulation method for audio signal modules, it is advisable to fine-tune the software/hardware interface. This involves hardware calibration using the analog potentiometers integrated into the ADC and software calibration within the VGE system by adjusting time delays through the "Delay" block. Therefore, the optimal configuration for using the cyber-physical emulation method with SPICE models in real-world applications involves a sampling frequency of 44.1 kHz, a buffer size ranging from 512 to 1024 samples, and the ASIO data I/O protocol.

Authors' contributions

N.R. Levchenko developed a plugin for cyber-physical simulation, conducted experiments, and processed findings.

M.S. Kostin suggested a cyber-physical approach to analyzing audio signal modules, offering guidance on conducting and interpreting experimental findings.

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