Micro- and nanoelectronics. Condensed matter physics

Микро- и наноэлектроника. Физика конденсированного состояния

UDC 621.382.3
https://doi.org/10.32362/2500-316X-2025-13-2-57-73
EDN TTUFNR

REVIEW ARTICLE

Thermal and mechanical degradation mechanisms in heterostructural field-effect transistors based on gallium nitride

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Abstract

Objectives. Gallium nitride heterostructural field-effect transistors (GaN HFET) are among the most promising semiconductor devices for power and microwave electronics. Over the past 10–15 years, GaN HFETs have firmly established their position in radio-electronic equipment for transmitting, receiving, and processing information, as well as in power electronics products, due to their significant advantages in terms of energy and thermal parameters. At the same time, issues associated with ensuring their reliability are no less acute than for devices based on other semiconductor materials. The aim of the study is to review the thermal and mechanical mechanisms of degradation in GaN HFETs due to the physicochemical characteristics of the materials used, as well as their corresponding growth and post-growth processes. Methods for preventing or reducing these mechanisms during development, production, and operation are evaluated.

Methods. The main research method consists in an analytical review of the results of publications by a wide range of specialists in the field of semiconductor physics, production technology of heteroepitaxial structures and active devices based on them, as well as the modeling and design of modules and equipment in terms of their reliable operation.

Results. As well as describing the problems of GaN HFET quality degradation caused by thermal overheating, mechanical degradation, problems with hot electrons and phonons in gallium nitride, the article provides an overview of research into these phenomena and methods for reducing their impact on transistor technical parameters and quality indicators.

Conclusions. The results of the study show that strong electric fields and high specific thermal loading of high-power GaN HFETs can cause physical, polarization, piezoelectric and thermal phenomena that lead to redistribution of mechanical stresses in the active region, degradation of electrical characteristics, and a decrease in the reliability of the transistor as a whole. It is shown that the presence of a field-plate and a passivating SiN layer leads to a decrease in the values of mechanical stress in the gate area by 1.3–1.5 times. The effects of thermal degradation in class AB amplifiers are more pronounced than the effects of strong fields in class E amplifiers; moreover, the mean time to failure sharply decreases at GaN HFET active zone temperatures over 320–350°C.

Keywords: GaN HFET, heterostructure, dual-channel HFET, coupled-channel HFET, current, self-heating, thermal conductivity, degradation, doping

• **Submitted:** 14.05.2024 • **Revised:** 12.07.2024 • **Accepted:** 11.02.2025

For citation: Minnebaev V.M. Thermal and mechanical degradation mechanisms in heterostructural field-effect transistors based on gallium nitride. *Russian Technological Journal.* 2025;13(2):57–73. https://doi.org/10.32362/2500-316X-2025-13-2-57-73, https://elibrary.ru/TTUFNR

Financial disclosure: The author has no financial or proprietary interest in any material or method mentioned.

The author declares no conflicts of interest.

ОБЗОР

Тепловые и механические механизмы деградаций в гетероструктурных полевых транзисторах на нитриде галлия

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Резюме

Цели. Гетероструктурные полевые транзисторы на нитриде галлия (GaN HFET, heterostructural field-effect transistor) являются наиболее перспективными полупроводниковыми устройствами для силовой и сверхвысокочастотной электроники. За последние 10–15 лет GaN HFET прочно заняли место в аппаратуре радиоэлектронных средств передачи, приема и обработки информации, а также в изделиях силовой электроники за счет существенных преимуществ в энергетических и тепловых параметрах. При этом вопросы обеспечения их долговременной надежности стоят не менее остро, чем для приборов на других полупроводниковых материалах. Целью исследования является обзор тепловых и механических механизмов деградаций в GaN HFET, обусловленных физико-химическими особенностями применяемых материалов, ростовыми и пост-ростовыми процессами, и способов купирования этих механизмов при разработке, производстве и эксплуатации.

Методы. Основным методом исследования является аналитический обзор результатов публикаций широкого круга специалистов в области физики полупроводников, технологии производства гетероэпитаксиальных структур и активных приборов на их основе, моделирования и проектирования модулей и аппаратуры, надежности и эксплуатации.

Результаты. Описаны причины снижения показателей качества GaN HFET, вызываемые тепловыми перегревами, механическими деградациями, проблемами с горячими электронами и фононами в нитриде галлия, а также представлен обзор исследований, посвященных этим явлениям и методам снижения их воздействия на технические параметры транзисторов и показатели качества.

Выводы. По итогам исследования отмечено, что сильные электрические поля и высокая удельная тепловая нагруженность мощных GaN HFET вызывают физические, поляризационные, пьезоэлектрические и тепловые явления, способные приводить к перераспределению механических напряжений в активной области, деградации электрических характеристик и снижению надежности транзистора в целом. Установлено, что наличие полевой платы и пассивирующего слоя из нитрида кремния SiN приводят к снижению значений механических напряжений в области затвора в 1.3–1.5 раз, эффекты тепловой деградации в усилителях класса AB выражены сильнее, чем эффекты воздействия сильных полей в усилителях класса E, при температуре активной зоны GaN HFET более 320–350 °C резко снижается время средней наработки до отказа.

Ключевые слова: GaN HFET, гетероструктура, двухканальный HFET, HFET со связанными каналами, ток, саморазогрев, теплопроводность, деградация, легирование

• **Поступила:** 14.05.2024 • **Доработана:** 12.07.2024 • **Принята к опубликованию:** 11.02.2025

Для цитирования: Миннебаев В.М. Тепловые и механические механизмы деградаций в гетероструктурных полевых транзисторах на нитриде галлия. *Russian Technological Journal*. 2025;13(2):57–73. https://doi.org/10.32362/2500-316X-2025-13-2-57-73, https://elibrary.ru/TTUFNR

Прозрачность финансовой деятельности: Автор не имеет финансовой заинтересованности в представленных материалах или методах.

Автор заявляет об отсутствии конфликта интересов.

INTRODUCTION

The achievements of recent years in the development of power and high-power microwave devices are mainly associated with III-nitride materials and the various devices based on them [1–3]. Heterostructured field-effect transistors (HFET) on gallium nitride (GaN) are the most promising for high-power microwave and power applications due to the sufficiently high mobility of electrons, high density of charge carriers, and high breakdown voltages, which is especially evident when operating in pulsed modes [4].

The idea of charge accumulation at the interface of a heterojunction first proposed in the late 1960s led to the possibility of creating an amplifying device on this basis. However, it was only after the development of high-quality high-precision epitaxial growth methods in the 1970s that the task of transforming a field-effect transistor (FET) into a heterostructural field-effect transistor (HFET)—also known as a high electron mobility transistor (HEMT)—could be solved [5].

In 1978, the achievement of high electron mobility obtained by modulating doping was demonstrated for the first time; in 1980, the University of Illinois demonstrated a device called a modulated-doped field-effect transistor (MODFET). During the following decades, the efforts of engineers and scientists from different countries led to more complex devices such as double heterojunction field-effect transistors [6]. The simplest GaN/AlGaN HFET structure incorporating aluminum–gallium nitride AlGaN is shown in Fig. 1 [7]. AlN/AlGaN/GaN/AlGaN/GaN/AlGaN multilayer heterostructures have become the basis for a new component base of solid-state microwave electronics.

The above-described structure is not the only possible one for GaN HFETs. For example, in InAlN/AlN/GaN devices incorporating indium-aluminum nitride (InAlN), a different structure is used for this purpose. Although both structures exhibit polarization, the AlGaN variety has stronger piezoelectric polarization, whose effect can be enhanced due to structural characteristics. For example, the piezoelectric effect is stronger in GaN/AlGaN than in InAlN/AlN due to the grid mismatch between the layers [8]. Here, the spontaneous polarization for the InAlN/AlN/GaN structure plays

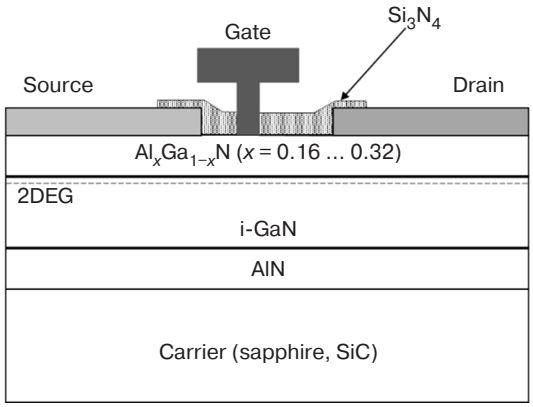


Fig. 1. The simplest structure of GaN/AlGaN HFET. 2DEG is two-dimensional electron gas; AlN is a buffer layer of aluminum nitride minimizing differences in step parameters of the chip lattice of heterostructure and carrier; SiC is a silicon carbide carrier

the only role except when the aluminum nitride (AlN) interface layer is used [9].

HFETs can be categorized into three main types depending on the GaN/AlGaN structure (Fig. 2). The typical structure, which consists of a single two-dimensional electron gas (2DEG) channel, is classical only because other HFET structures are often compared to it when evaluating the improvement of properties.

A typical HFET structure starts with a layer of AlN grown on a carrier (Al_2O_3, SiC, Si) followed by a thicker GaN buffer layer. The reason for using GaN on AlN (grid mismatch) is due to the first buffer layers serving as semi-isolating layers. After GaN growth, the growth of the AlN separating layer continues. Since the high frequency performance of AlGaN/GaN HFET is degraded due to the transfer of high-energy electrons from GaN to the AlGaN barrier, the AlN layer needs to be grown in between them to prevent high-energy electrons from moving to the AlGaN layer, thus keeping the electrons in GaN and creating a high-density 2DEG. However, this layer should not be thick (typically about 2 nm) due to the grid mismatch between GaN and AlN, which causes strain relaxation and cracking [10]. This layer is used to better confine the 2DEG channel due to the wider bandgap due to the penetration of electrons into the barrier material actually changing the effective

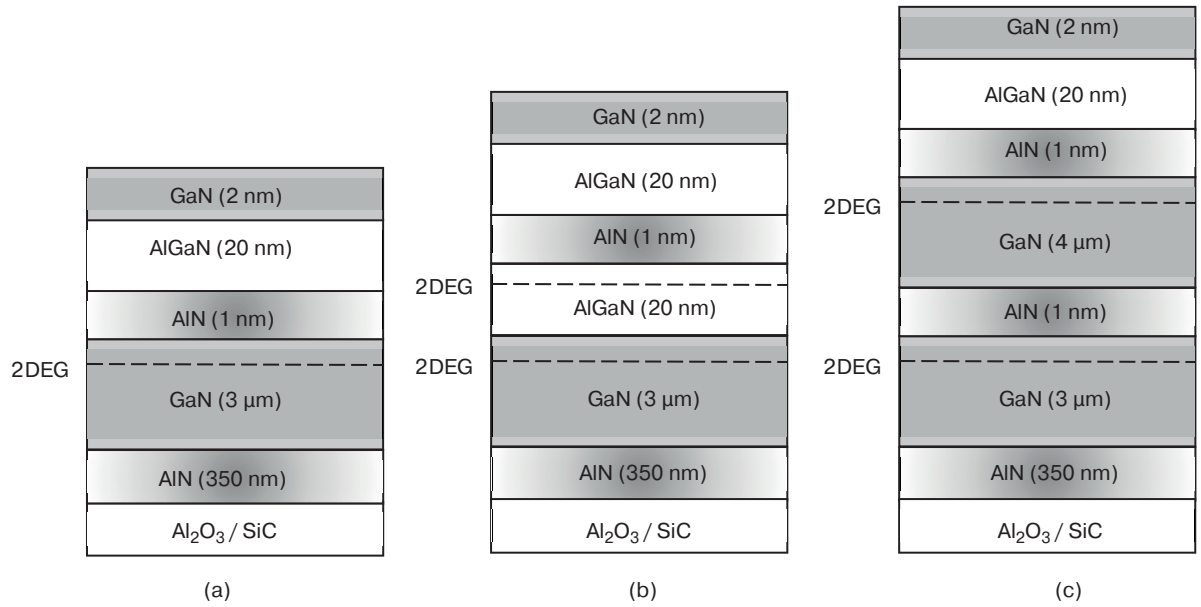


Fig. 2. Conventional schematic representation of GaN HFET heterostructure: (a) single-channel (classical), (b) dual-channel, (c) coupled-channel

mass and electron scattering rate. AlGaN is then grown in such a way as to force electrons to form a channel in GaN that relies on the polarization difference between it and the GaN layer below. A final 2-nm thick GaN layer is used to protect the AlGaN from oxidation and provide a better metallic contact to GaN than to AlGaN. The corresponding structure is depicted in Fig. 2a.

Another type of structure used for HFETs is the dual-channel HFET (Fig. 2b), which has a higher electron density. The third type of HFET structure, shown in Fig. 2c, is the coupled-channel HFET. In this structure, unlike the two-channel structure, the two channels are at the same energy level, so they can be coupled to form a channel called a three-dimensional electron gas or 3DEG.

1. SOURCES AND MECHANISMS OF GaN HFET FAILURES

Due to the strong electric fields present in GaN HFETs, as well as the interaction of thermal, physical, polarization fluxes, etc., there are multiple degradation paths in HFETs caused by overheating, resulting in a decrease in specific current, as well as an increase in gate leakage current and reliability limitations. Power dissipation associated with hot electron-hot phonon interactions can be caused by several mechanisms. A number of papers have investigated these degradation mechanisms and described approaches for reducing their deleterious effects. Depending on the operating time of a semiconductor device, there are three main failure periods (Fig. 3) [11]. As can be seen, the presence of device failure does not depend on the time of its operation; thus, designers strive to exclude failures at stages *I* and *II*, as well as to maximize their reduction at the aging period.

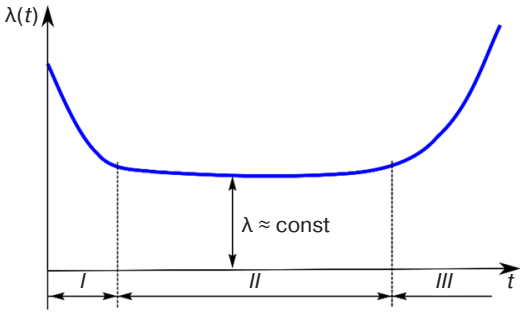


Fig. 3. Typical dependence of failure intensity λ on operation time *t*: *I* is a period of running-in and failures of low-quality products; *II* is a period of normal operation (failure intensity is approximately constant); *III* is a period of aging (failures are caused by wear and/or aging of materials)

In order to describe the above-mentioned degradations, let us define their mechanisms. Although it is rather difficult to classify all degradation mechanisms, for better understanding we will divide them into three main groups: electrical, thermal and mechanical. These mechanisms and their interrelation are shown in the so-called "magic triangle" of interactions that demonstrates the connections between electrical, mechanical, and thermal interactions (Fig. 4) [7].

We will discuss the location of the main sources of transistor failures typically manifested during operation (Fig. 5) on the example of the simplest GaN/AlGaN HFET structure.

From Figs. 4 and 5, it can be seen that the failure mechanisms in GaN HFETs are closely related. Here, failure sources *1* and *4* are peculiar to GaN devices due to the presence of spontaneous and piezoelectric polarization fields in AlGaN/GaN heterostructures,

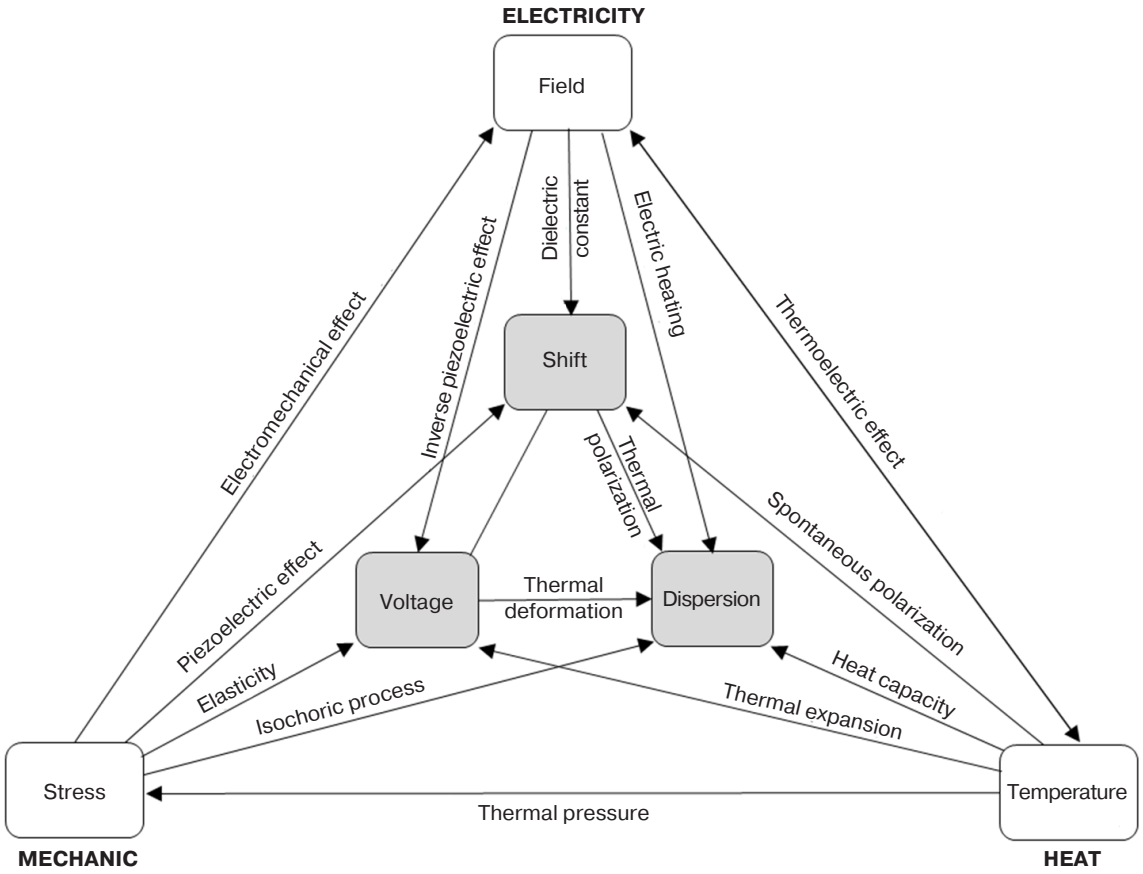


Fig. 4. "Magic triangle" of interactions

while sources *2* and *3* are caused by the presence of hot electrons occurring at high supply voltage levels, and sources *5–8* are activated by temperature increase [13].

The issues related to reliability improvement and approaches to solving them require understanding of GaN HFET degradation mechanisms, which can pose a serious problem due to the peculiarities of GaN device physics and imperfections of initial materials, as well as growth and post-growth processes of device fabrication. It was noted in [14–18] that some degradation effects occur even when the devices are in the off state (without bias voltages applied) or during double-state Schottky gate biases [14–18]. In this case, the most significant manifestation of degradation is a catastrophic increase in gate current leakage. The existence of a critical voltage above which degradation of GaN HFET parameters occurs led to the proposal of a degradation mechanism based on the formation of defects due to the inverse piezoelectric effect [13]. Failure mechanisms *5–8* refer to heat-activated degradation mechanisms, which were previously also observed in devices built on other semiconductor materials (Si, GaAs, InP, SiC, etc.). This suggests that these failure mechanisms are more related to metallization technologies and materials rather than to gallium nitride itself [13], but can be more pronounced in the latter due to the peculiarities of growth and post-growth technologies.

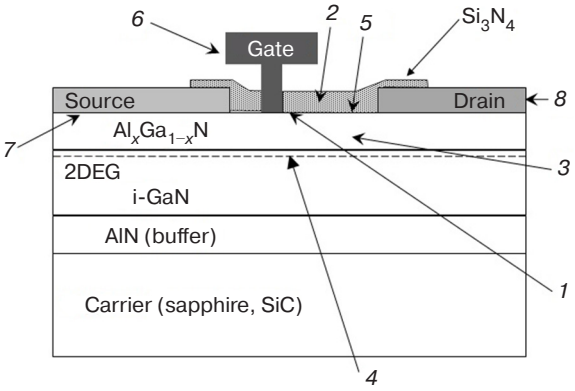


Fig. 5. Main identified failure mechanisms [12]:
(*1*) electric field causing degradation of the gate edge and pre-existing temperature defects;
(*2*) trapping of electrons in the passivation layer;
(*3*) generation of traps by hot electrons;
(*4*) generation of traps due to electrothermomechanical damage (temperature; electric field; mechanical deformation);
(*5*) thermally induced delamination of passivation;
(*6*) degradation of metal connection with the gate due to electrothermomechanical damage caused by traps;
(*7*) degradation of interlayer connections;
(*8*) degradation of ohmic contacts

Electrical mechanisms of GaN HFET degradation are discussed in detail in [19]. Now let us proceed to the analysis of thermal and mechanical failure mechanisms, as well as their interrelation with electrical mechanisms.

2. THERMAL MECHANISMS OF GaN HFET DEGRADATION

A. The problem of self-heating

When the chip grid of a semiconductor material cannot fully dissipate the heat generated by hot electrons through the emission of hot LO phonons[1], this excess heat accumulates in the structure, interacts with hotter electrons and causes even more heat, while there is no effective dissipation mechanism. Consequently, the temperature of the device rises, resulting in degraded device performance. This mechanism, called self-heating, is an important problem for GaN HFETs operating at high currents and powers.

In [20], the self-heating phenomenon of AlGaN/GaN HFETs was investigated using sapphire or SiC as a substrate. It is observed that in AlGaN/GaN HFETs grown on 6H-SiC substrates, the allowable maximum power dissipation is at least 3 times higher than that of those grown on sapphire under the same conditions. This is a result of the higher thermal conductivity of 6H-SiC compared to sapphire. However, the problem with using SiC as a carrier is its high cost. In order to understand better the effect of self-heating, we present the simulation results of temperature change in AlGaN/GaN HFETs with different geometry, heterostructure design, doping density, and substrate type obtained in [21].

In order to calculate the temperature rise, the authors started with the nonlinear flow equation and continued the simulation in doped and undoped AlGaN/GaN HFET channels on SiC. The structure used for the simulation and the simulation result are shown in Figs. 6 and 7, respectively [20]. It can be seen from the figures that the sample with undoped GaN 2DEG channel layer dissipates heat to a significantly lower extent compared to the sample with doped GaN channel layer.

It is known from solid state physics that there are two mechanisms that contribute to heat conduction. Thermal conduction can result from vibration of grid nodes as well as electronic conduction. The grid contribution to the thermal conductivity of pure chip s is defined by the expression:

$$k_{\text{grid}}(T) = \frac{1}{3} V_s C_{\text{grid}}(T) L(T), \qquad (1)$$

where T is the temperature, V_s is the speed of sound in the semiconductor, $C_{\text{grid}}(T)$ is the grid heat capacity, and $L(T)$ is the average phonon free path length.

[1] LO Phonon is a longitudinal optical phonon in semiconductor chips.

The contribution of electronic conduction to thermal conductivity is negligible at doping concentrations less than 10^{19} cm^{-3}. On the other hand, since penetrating dislocations decrease V_s and increase phonon scattering, the thermal conductivity of material decreases due to an increase in the dislocation density (GaN as a pure material has a much higher thermal conductivity compared to epitaxial GaN layers). At the same time, the increase in phonon scattering due to the increase in doping concentration dominates over the increase in the contribution of electronic conduction.

Consequently, the thermal conductivity decreases by increasing the doping concentration (k_{grid} decreases by a factor of about 2 for each decade of increasing n concentration), which is consistent with the findings of [20, 22].

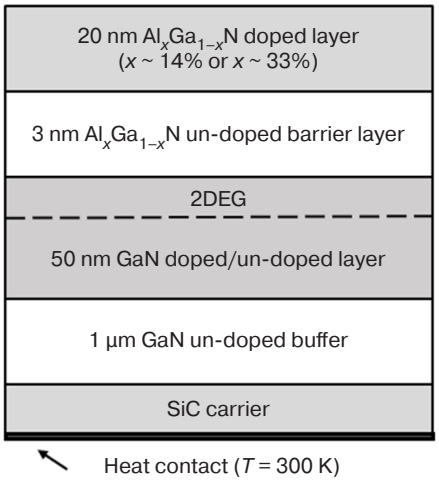


Fig. 6. Structure of the doped/undoped HFET used in [20]

In [21], it is shown that with a greater increase in temperature, the electron mobility begins to decrease. In addition, when the size of the transistor decreases, the negative effect of doping becomes even more pronounced due to an increase in the density of dislocations and an increase in the relative number of defects due to size reduction.

B. Degradations associated with heat exposure

In order to identify a specific device degradation effect, it is necessary to define the test conditions in such a way that other degradation mechanisms do not affect the results obtained. When the gate is reverse biased (the transistor is "locked"), the drain current is very small and therefore, as the temperature increases, it can be assumed that there are no other effects in the channel than the applied thermal energy. In this way, the degradation effects caused by thermal effects can be monitored. By applying this test condition to GaN HFETs, it is possible

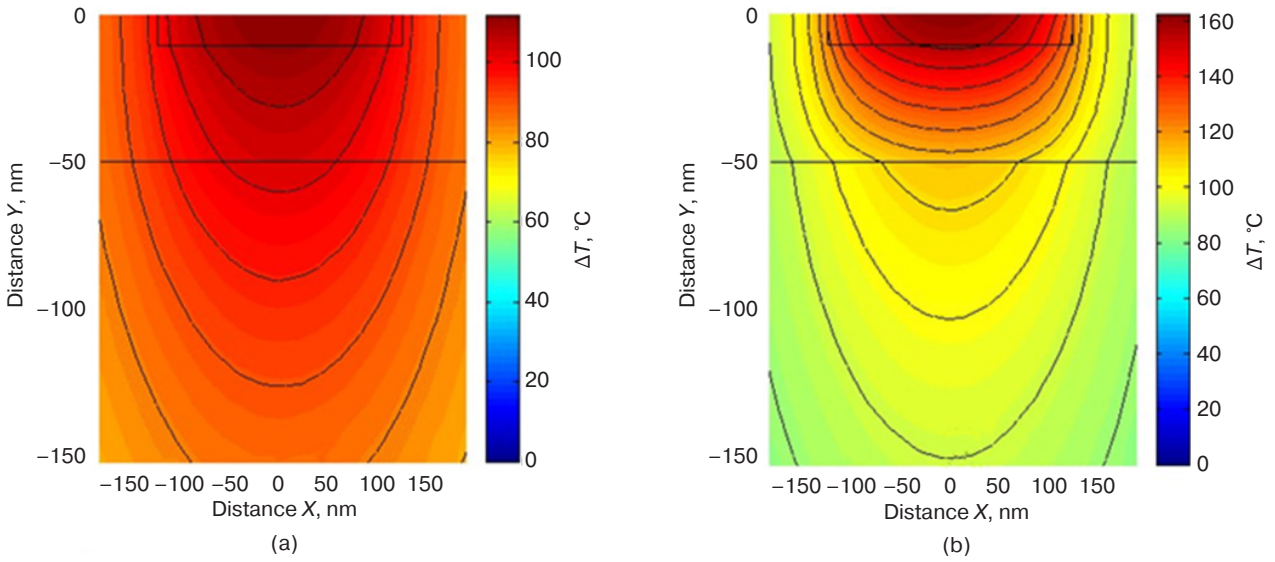


Fig. 7. Temperature rise profile in undoped (a) and doped (b) AlGaN/GaN HFET channels grown on SiC carrier [20]

to understand how thermal energy is dissipated in the channel.

Thermal scattering is related to the thermal conductivity of the material. It is known that the more acoustic phonon modes are occupied in the structure of a semiconductor, the greater its thermal conductivity. It was shown in [23] that the group velocity of acoustic phonons is much higher than that of optical phonons. Consequently, at low temperatures, optical phonon modes are not occupied, but only acoustic phonon modes are occupied. However, this is only true for small electric fields, which is usually not the case in high-power HFETs unless measurements are made at very small drain and gate biases. It can also be said that according to (1), at low temperatures the free path length L is relatively large and is dominated by the finite chip size (size effect), the number of defects (negligible in the case of a pure chip) and the thermal conductivity of the grid $C_{\text{grid}}(T) \sim \left(\frac{T}{\theta_D}\right)$, where θ_D is the Debye temperature. With increasing temperature, the thermal conductivity of the grid $C_{\text{grid}}(T)$ first begins to saturate, and at very high temperatures the thermal conductivity drops due to phonon–phonon and phonon–electron scattering processes [20] (Fig. 8).

In the study [24], various research methods such as Raman micro-thermography, micro-photoluminescence spectroscopy and thermal modeling have been applied to better understand the thermal properties of AlGaN/GaN HFETs. It is confirmed that the thermal conductivity is higher in bulk GaN than epitaxial layers due to the fact that the bulk material has lower dislocation density. At the same time, if the quality of bulk GaN is good enough, the epitaxial layers will also be of higher quality, other things being equal. It is proved that the thermal resistance in GaN-on-SiC is very close to that of GaN-on-GaN, although GaN has a slightly lower thermal conductivity of C_{GaN} ~ 260 W/(m·K) for bulk GaN compared to C_{SiC} ~ 480 W/(m·K) for SiC. The reason may be due to the lack of thermal boundary resistance between the device layers and the substrate [24]. Figure 9 shows the surface temperature and depth profile at the center of a 30 × 80 μm AlGaN/GaN HFET calculated in a 3D simulator and measured by photoluminescence and Raman micro-spectroscopy. Using Fig. 9 and the assumption of zero thermal boundary resistance (TBR_{eff}) at the GaN–GaN interface and uniform GaN thermal conductivity, as well as approximating the measured curve using the 3D-T thermal model with a standard thermal conductivity temperature dependence $T^{-1.22}$,

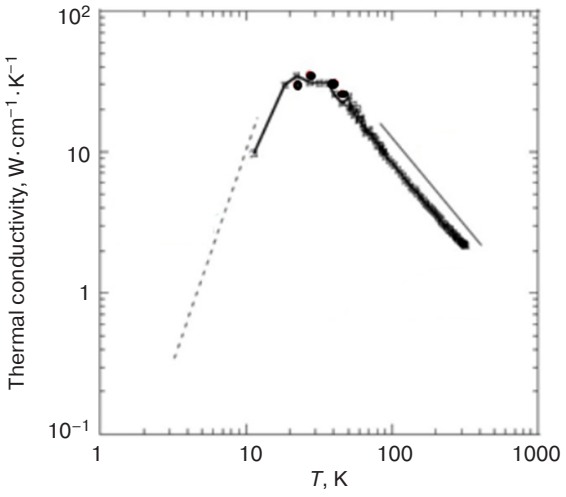


Fig. 8. Temperature dependence of thermal conductivity of GaN HFET with gate width W_g = 200 μm: dashed line—scattering limit at phonon free path length of 500 μm due to size effect, solid line—dependence $T^{-1.22}$ [20]

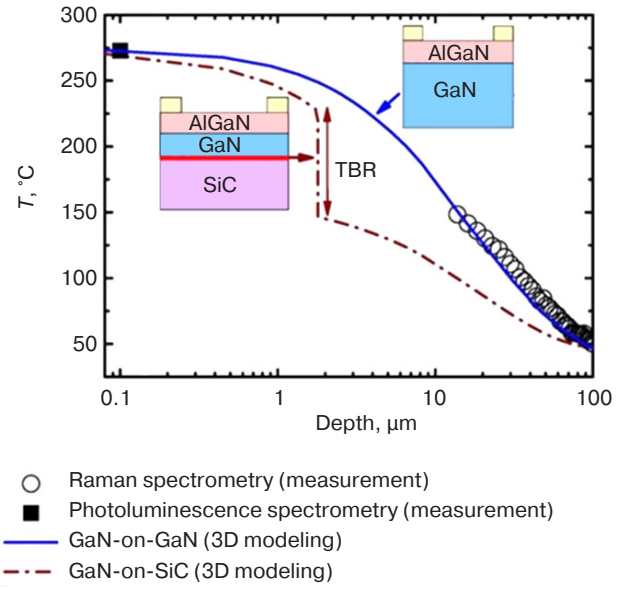


Fig. 9. Dependence of temperature T on the surface on the substrate thickness [24]

we obtain a C_{GaN} thermal conductivity C_{GaN} ~ 260 W/(m·K), in contrast to the thin epitaxial layer having a value C_{epiGaN} ~ 150 W/(m·K).

In [25], a developed ML-TCAD[2] coupled electronic model is presented, which enables prediction of the gain reduction and efficiency of GaN HEMTs induced by hot electron effects and does not require knowledge of reliability physics and results of long-term experimental tests. The resulting model predicts with high reliability the results of drain current variation in GaN HEMTs under the effect of hot electron voltage. In addition, the model allows us to determine the location, distribution, concentrations, and energy levels of traps in GaN HEMT from the current–voltage degradation curves, which is certainly useful for further studying the physical degradation mechanism of GaN HEMT under hot electron exposure.

C. Degradation of ohmic contacts and passivation coatings

AlGaN/GaN HFETs use ohmic contacts with standard gold metallization, which seems to guarantee sufficient stability under elevated temperature tests up to a certain limit. In [24], GaN HFETs with Ti/Al/Pt/Au ohmic contacts were subjected to step voltage for 48 h. It was found that the ohmic contacts begin to degrade at transition temperatures above 300°C—self-heating of the transistor leads to degradation of performances of devices and blocks due to degradation of the ohmic contacts [13, 24].

In [26], the degradation of AlGaN/GaN/SiC HFETs with 25 μm gate length and different passivation coatings related to the temperature regime of transistor operation was investigated. It was shown that the threshold voltage degradation starts in the temperature range of 310–330°C. Changes in the structure of the transistor were analyzed by measuring electroluminescence and using transmission electron microscopy (TEM). The formation of voids and gold diffusion in AlGaN/GaN were detected. These processes are responsible for device degradation with conventional passivation techniques.

The temperature increase of the active region and the transistor chip itself depends, among other things, on the choice of the operating point and the level of input microwave power. Figure 10 shows the thermal distribution over the chip surface in the input-to-output cross section of an AlGaN/GaN/SiC HFET with overall dimensions of 480 × 800 × 100 μm, gate length L_G = 25 μm, and gate width W_G = 6 × 200 μm. The tests were performed at a case base temperature of 120°C.

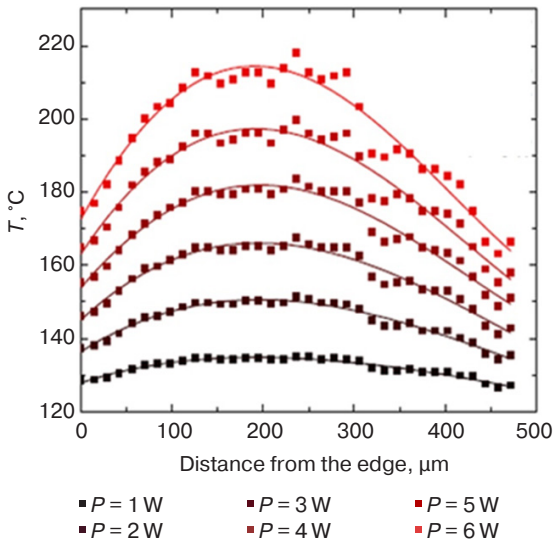


Fig. 10. Temperature distribution T on the chip surface at different power levels of the input microwave signal [26]

It can be seen that when the power load P is increased, the temperature distribution over the transistor area changes dramatically. The resulting temperature nonuniformity will certainly be the cause of subsequent transistor failures. Additional studies confirm that the temperature increase of the chip surface depends both on the case temperature and power dissipated (Fig. 11).

It is found that when exposed to elevated temperature, the gate current increases and the gate threshold voltage shifts to the negative side, and this is due to the passivation layers.

[2] ML-TCAD is an electronic model of a transistor created on machine learning (ML) basis to significantly speed up calculations in the TCAD (Technology Computer-Aided Design) environment by minimizing physical calculations.

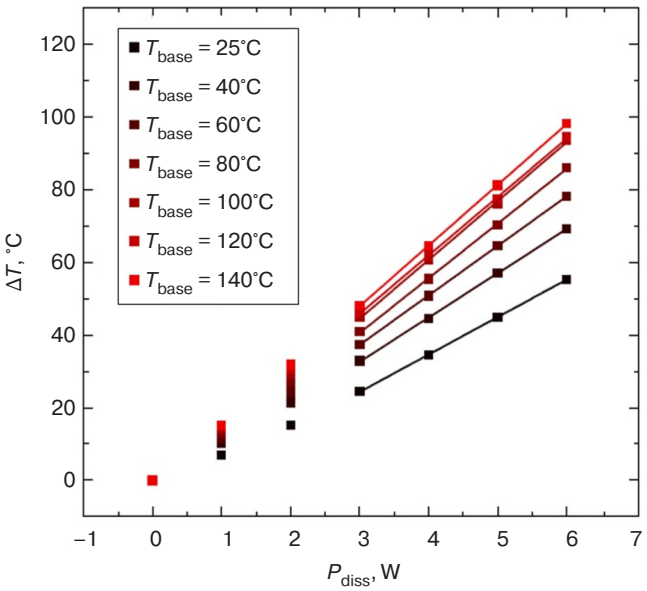


Fig. 11. Dependence of transistor surface temperature increment ΔT on power dissipation P_{diss} at different base temperatures [26]

In [27], the results of investigation of microscopic origin of the vulnerability of GaN HFET materials and devices based on them to high temperatures by monitoring the onset of structural degradation at different temperature conditions in real time are presented. The studies have been carried out by means of SEM. Electron-transparent samples were fabricated from bulk material and heated up to 800°C. High-resolution transmission electron microscopy, scanning transmission electron microscopy, energy-dispersive X-ray spectroscopy, and geometric phase analysis (GPA) were performed to assess the quality of chips, to study the diffusion of materials and the processes of strain propagation in the sample before and after heating. It was observed that the decrease of the gate contact area is noticeable starting from the temperature 470°C, and it is accompanied by Ni/Au mixing near the gate/AlGaN interface. Elevated temperatures cause significant out-of-plane lattice expansion at the SiNx/GaN/AlGaN interface, as shown by GPA strain maps with geometric phase, while in-plane strain remains relatively constant. In this study, it is shown that exposure to temperatures exceeding 500°C leads to 2 orders of magnitude increase in leakage current in GaN HFETs. The results of this study provide real-time visual information to determine the initial location of degradation and highlight the effect of temperature on GaN HFET structure, its electrical properties, and material degradation.

D. Failure and service life testing

Thermal effects are one of the major problems that reduce the performance and reliability of a semiconductor device. It is the most common mechanism because AlGaN/GaN HFETs mainly operate at relatively high temperatures.

Device reliability is a very important issue. Nowadays, every company has separate departments that focus on the quality and reliability of their devices. For any manufactured devices, it is required to determine the area of safe operation, the average time until failure, and the shelf life of devices and appliances. Therefore, the industry pays great attention to the reliability of its products—samples are subjected to numerous tests, including short-term and long-term failure and survivability. As you can understand from the name, these tests are conducted to evaluate the service life of the device. Since you cannot wait 10 or 25 years to see what happens to a semiconductor device, special conditions are applied to conduct relatively short time tests to evaluate the mean time to failure (MTTF).

These accelerated life tests are basically performed at three different temperatures and for each one the MTTF is measured. By extrapolating these values to the temperature at which the device is operating (with the device junction temperature being higher than the case temperature), the MTTF for the device can be obtained. Figure 12 shows how the MTTF is evaluated in a failure test: the MTTF is measured at three junction temperatures of 260, 285, and 310°C, and by extrapolation it is determined that at an operating junction temperature of 150°C the MTTF is more than 10^7 h, activation energy E_a = 2.0. Usually, the minimum possible number of devices is tested, but in such a way that the measurements do not lose accuracy [7].

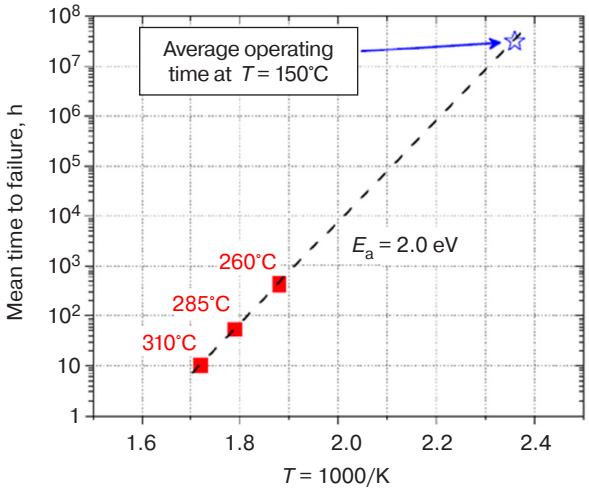


Fig. 12. Determination of MTTF by measurement at three temperatures

At the permissible operating temperature of the *p-n*-junction *Tj* of the active zone of the GaN HFET chip, equal to 200°C, the average MTTF is 10^5 h (11.57 years). The device resistance to load mismatch up to a voltage standing wave factor of 10 in the large-signal mode is also demonstrated.

Rapid (within several hours) destruction occurs in modern GaN heterotransistors at junction temperatures of 320–350°C [13].

In [28], the degradation effects observed in GaN HFETs with a gate length of 0.15 μm were experimentally investigated under real power amplifier conditions, i.e., when a high-level microwave power is applied to the input. The measurements were performed for a series of devices in the loud-pull measurement mode. Consequently, this mode of experimentation provides information relevant to microwave signal operation and enables preferentially detecting changes in electrical quantities that cannot be directly detected at current–voltage curve or high frequencies. Values such as gate resistance now play a fundamental role in reliability analysis of technologies. Experiments were performed on GaN HFETs with the same gate width while operating in class AB mode, a saturation mode that emphasizes degradation effects caused by high temperatures due to increased power dissipation, and in class E mode, where degradation is enhanced by strong electric fields. Experiments were conducted at $T_1 = 23$°C and $T_2 = 100$°C. As a result, it is found that:

- GaN HFET degradation level depends on the actual radio frequency mode;
- thermal degradation effects, which are enhanced in the class AB mode, are more pronounced than the effects of strong fields in the class E mode;
- characterization of GaN HFETs under real microwave loads should be used to accurately and deeply investigate degradation and failure mechanisms in order to determine MTTF in practical microwave applications.

3. MECHANICAL MECHANISMS OF GaN HFET DEGRADATION

A. Inverse piezoelectric effect

Mechanical stresses are also important as part of the triangle of interactions (Fig. 4). Mechanical stresses have an important influence on the parameters and reliability of microwave GaN HFETs. Gallium nitride is a polar material, i.e., valence electrons are not distributed between two neighbors uniformly—this causes local polarization of the semiconductor chip. However, globally the polarization vector of GaN is zero. Consequently, when mechanical pressure is applied, the chip structure can bend or expand (depending on the direction of the force) and cause a resultant polarization that can act as an electric field. This phenomenon is called the piezoelectric effect.

On the other hand, if we apply an electric field to this chip, the chip can again bend or expand (depending on the direction of the electric field). In this case, the electric field induces a mechanical force—this effect is called the inverse piezoelectric field. When the gate–source voltage $U_{g.s.}$ is applied, the inverse bias of the gate channel becomes more and more depleted. If too large an electric field is applied in the direction opposite to the relaxation direction of the chip, it will induce a large mechanical force and may cause mechanical damage to the chip. Such an effect is what is called the inverse piezoelectric effect. This is what happens to GaN when too large a voltage $U_{g.s.}$ is applied.

Fabrication processes and operating conditions also affect mechanical stresses. In [29], in particular, the relationship between mechanical stresses and reliability of gallium nitride heterotransistors is discussed. In this work, $Al_{0.2}Ga_{0.8}N$(20 nm)/GaN(2 μm) structures on a 75-μm thick carrier were investigated. The calculations show that a 100-nm thick SiN passivation layer creates a mechanical stress of up to 300 MPa at the gate junction [13]. Tensile stresses are critical from the point of view of transistor reliability due to the fact that they contribute to the formation of "pits" on the surface of the heterostructure. Figure 13 shows the calculated value of mechanical biaxial stresses in the gate region as a function of specific power dissipation $P_{diss.sp.}$ for two GaN HFET designs:

- traditional—without SiN passivation coating and field-plate;
- improved—in the presence of SiN and field-plate, usually used to increase breakdown voltages in HFETs.

The given data show that the presence of the field board and SiN layer leads to a 1.3–1.5-fold reduction of mechanical stresses in the gate region depending on the specific power dissipation. Of course, mechanical stresses depend on both the substrate temperature and the temperature of the *p-n*-junction.

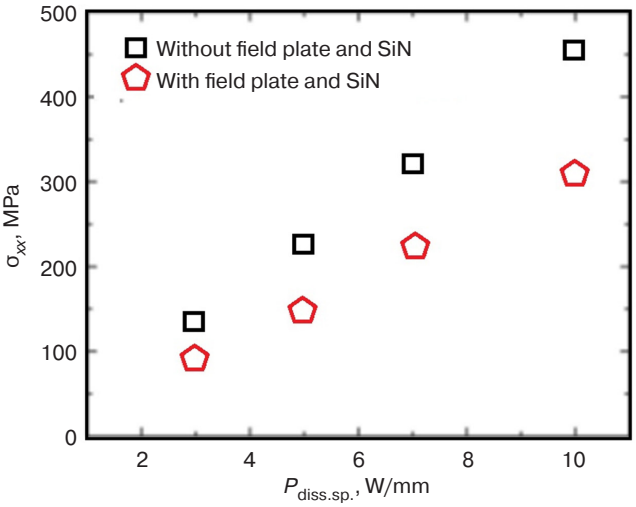


Fig. 13. Dependence of the magnitude of mechanical biaxial stresses σ_{xx} on the specific power dissipation $P_{diss.sp.}$ in GaN HFET [13]

In [29], calculations of the values of mechanical biaxial stresses σ_{xx} in GaN HFETs arising due to the inverse piezoelectric effect (Fig. 14), the consequence of which is the appearance of the electric field. For comparison, Fig. 14 outlines the area corresponding to the values of the electric field strength arising in the transistor at voltages ($V_{d.s.}$) between the drain and source $U_{d.s.}$ = 50–70 V.

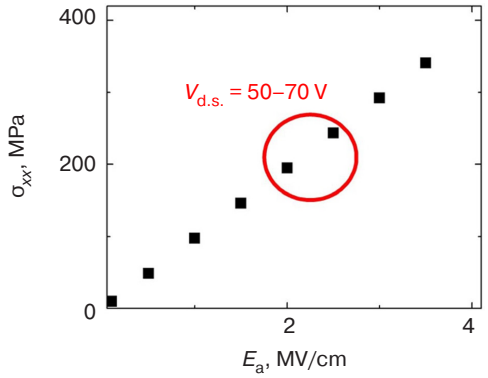


Fig. 14. Dependence of the magnitude of mechanical biaxial stresses σ_{xx} on the electric field strength in GaN HFET [29]

It follows from the data given in [29] that the values of the above mechanical stresses caused by the power dissipated in the transistor are comparable in magnitude to the stresses due to the inverse piezoeffect.

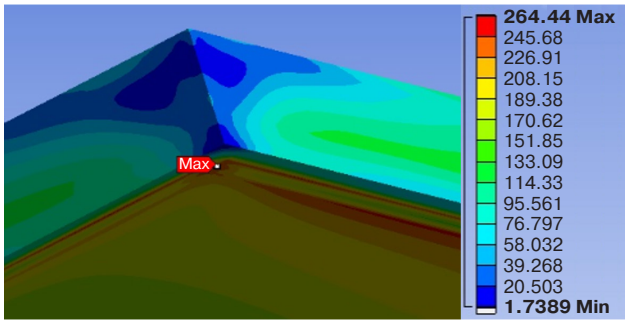
Ohmic contacts also create mechanical stresses. Thus, mechanical stresses in GaN heterotransistors are one of the reasons of their reliability decrease.

B. Interrelationship of thermal and mechanical degradation

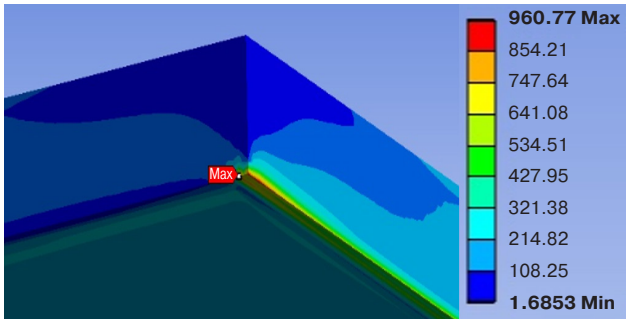
It was shown in [30] that the high specific thermal loading of high-power AlGaN/GaN/SiC transistors requires a particularly careful approach to heat dissipation in operating modes. Preventive measures to eliminate any assembly defects in high-power AlGaN/GaN/GiC transistors are essential. For example, the defect of vertical tilting of the chip after soldering it to the base leads to unequal thickness of the solder layer at the periphery between the chip and the base. The evaluation of stresses arising in the chip during heating depending on different variants of the chip arrangement in space, as well as their influence on the potential reliability of the chip structure are shown in [30], where the values and nature of the distribution of mechanical stresses in the chip were determined by calculating the stress–strain state of the chip model with a defect of displacement along the face or corner by the finite element method. The edge displacement in this case is a uniform increase/decrease in solder thickness between two parallel faces of the transistor chip, and the corner displacement is a change in solder thickness along the diagonal of the soldering plane.

Figure 15 shows the three-dimensional distribution of the main thermal stresses in the SiC layer. Based on the obtained values of equivalent stresses for the variants of chip position, the safety factor was calculated. The safety factor determines how much the actually designed structure can withstand the induced thermal stresses.

In [30], it is shown that the chip reliability of AlGaN/GaN/SiC transistors deteriorates by a factor of 6.5 at the maximum angle tilt and by a factor of 3.6 at the maximum edge tilt. Thus, it is shown that the displacement of the chip plane significantly increases mechanical stresses in the chip body in areas with thinning solder layer, which, in turn, means the potential development of mechanical failures of the structure, especially under cyclic thermal loads.



(a)



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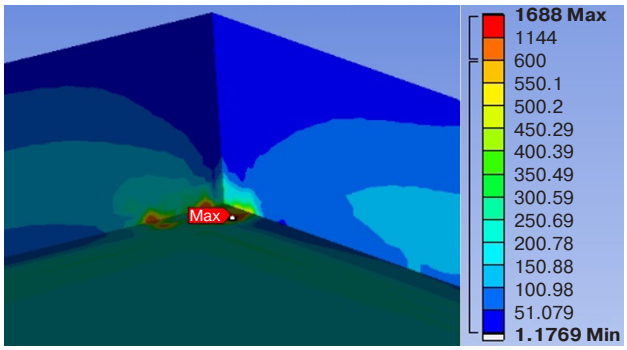


(c)

Fig. 15. Distribution of main stresses in the chip under continuous power dissipation for the case of:
(a) uniform constant solder thickness,
(b) nonconstant thickness along the face,
(c) nonconstant thickness along the angle [30]

C. Relationship between electrical and mechanical damage

Degradation may be reversible or irreversible. If the product returns to its normal state after the end of stress impact, we can talk about reversible degradation. However, sometimes after the end of degradation the device is irreversibly changed, which is interpreted as damage or irreversible degradation.

Electrical degradation is characterized by the value of critical applied voltage below which degradation is reversible. Application of voltages higher than the critical voltage causes irreversible degradation. In [31], significant crystallographic damage induced by strong electromagnetic fields is shown, as well as the correlation between electrical degradation (sudden drop in current consumption, current collapse, increase in gate leakage current, avalanche injection, etc.) and material degradation as a mechanical effect. To find the correlation between electrical and physical damage, the depth and width of pits for different samples are measured from images obtained by transmission electron microscopy. Then, a degradation plot of the percentage of saturation current $I_{d.s.sat}$ between drain and source and collapse current $I_{d.s.coll}$ values as a function of the depth of the defect region is plotted to obtain a quantitative comparison between electrical and mechanical damage. This is shown in Fig. 16 [32] and implies that these mechanisms are interrelated and crystallographic damage is responsible for electrical degradation.

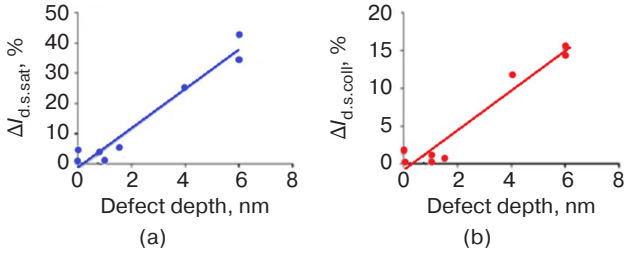


Fig. 16. Correlation between the values of $I_{d.s.sat}$, $I_{d.s.coll}$ and the depth of defects [32]

Figure 17 schematically shows the mechanical stress distribution in the gate region when a negative voltage is applied to the gate with respect to the drain and source [33].

When the transistor operates in pulsed mode, the mechanical stresses shown in Fig. 17 increase and decrease. While amplifiers based on microwave GaN HFETs should operate for 15–20 years, billions or even trillions of such cycles occur in the transistor. Eventually, a crack occurs in the gate region on the drain side. This is due to the fact that the tensile mechanical stresses on the drain side relative to the gate in operating mode when voltage is applied to the drain are greater than on the source side. In the initial stage of the process,

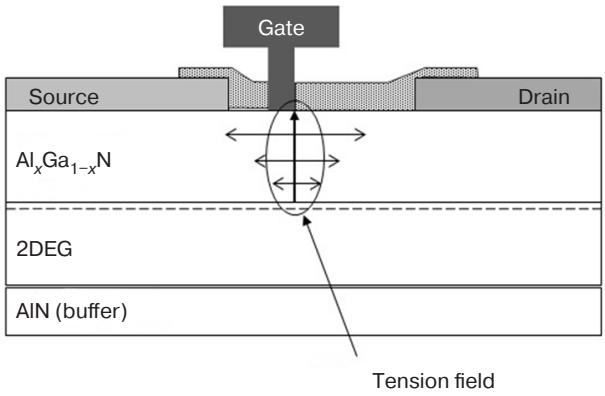
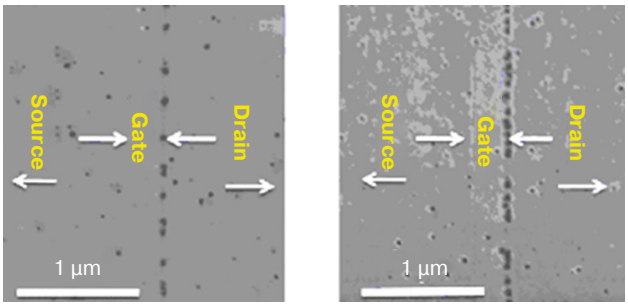


Fig. 17. Stretching regions of the AlGaN layer resulting from the inverse piezoelectric effect

defects in the form of pits are formed—less deep and rare on the source side and deeper and more frequent on the drain side. Figure 18 shows the time evolution of the process [34].



(a) (b)

Рис. 18. Evolution of crack formation from pitted defects in time [34]:
(a) after 10 min, (b) after 1000 min

Jimenez investigated the degradation mechanisms of a power amplifier in the form of a 3-stage microwave monolithic integral circuit (MMIC) W-band based on gallium nitride under the influence of an input microwave signal of high-power level[3]. The same experiments were performed on a discrete transistor with a gate periphery equal to the gate periphery of the MIC output stage. The studies did not reveal any shift in the threshold voltage (U_{thres}) after exposure to a high-power microwave signal; however, the modeled dynamic load lines showed that the output voltage fluctuations exceeded the breakdown voltage ($U_{d.s.break}$) when exposed to an input microwave signal with a high power level. Thus, it can be concluded from the experiment that the inverse piezoelectric effect will be the main factor of performance degradation, leading to defects and dislocations in the chip on the drain side.

[3] Jimenez J. *Advanced Reliability Aspects of GaN FETs*. Presented at European Microwave Week (EuMW), 2010.

Tsao et al. [35] confirms that the rather rapid development of gallium nitride-based power amplifiers, focused on high output power and efficiency, has created a critical problem for temperature control of devices in general. As a result of the thermal design and analysis of transistors and MMIC based on thermal maps measured by an infrared camera in continuous and pulsed modes of operation, it was found that the thermal resistance R_t "junction-to-case GaN-chip" at DC operation is 1.63°/W, and in pulsed mode R_t = 1.05°/W. Thus, it has been experimentally proved that to ensure the required reliability performance in the design of GaN MIC, only a thermal model reliably confirmed by functional testing should be used.

The presence of dislocation pits on the surface of the initial substrate leads to the subsequent formation of cracks [33]. Fine chemical treatment of its surface leads to the elimination or, at least, to the reduction of the formation of pitting. Foreign impurities (contaminants) also stimulate the degradation process. The double top layer of GaN ("cap") over the AlGaN barrier reduces the probability of subsequent degradation. These phenomena, which reduce the reliability of GaN HFETs, were taken into account in the developments of Cree[4] (USA) and UMS[5] (Germany) when developing microwave GaN HFETs for space applications [36].

The European Social Innovation Competition report (European high-quality GaN wafers on SiC substrates for space applications) reflects the following[6]:

- in order to improve the reliability and reduce the stresses shown in Fig. 17, the aluminum concentration in the barrier layer was reduced; the 22-nm thick barrier layer consists of an Al(16%)Ga(84%)N barrier and a 3-nm thick top protective GaN layer;
- layer carrier concentration in the 2DEG channel was slightly below $6 \cdot 10^{12}$ cm^{-2} (Cree) and below $3 \cdot 10^{12}$ cm^{-2} (SiCrystal). These values are typical values for HEMT structures with 18% Al (Cree) and 16% Al (SiCrystal) at 22-nm AlGaN barrier layer, respectively.
- average curvature value is 10.4 μm, average bend value is 4.96 μm.

It was shown in [37] that ultraviolet (UV) illumination very strongly reduces the breakdown voltage in GaN-on-Si, but this effect is negligible for GaN-on-SiC. Considering that the quality of the grown material is quite good (which may not be the case, especially for GaN-on-SiC), it can be assumed that UV illumination causes electrons to split and fall into traps due to the action of a field caused by the inverse piezoelectric effect. Therefore, this effect is more pronounced in GaN-on-Si due to the larger number of traps. In addition, this is another of the effects that confirm the correlation between the magnitude of the breakdown voltage of GaN HFETs and the number of traps in GaN, in other words, between electrical degradation and physical changes.

CONCLUSIONS

The strong electric fields present in GaN HFETs result in thermal, physical and polarization phenomena that degrade active element performance in the form of reduced specific drain current and increase gate leakage current and threshold voltage offset, as well as reducing breakdown voltages and specific output power and leading to lower reliability in general.

The redistribution of mechanical stresses in the chip due to the high specific thermal loading of high-power AlGaN/GaN transistors and consequent inverse piezoelectric effect results in mechanical damage of the structure and reduced reliability. However, the presence of the field board and SiN layer can reduce mechanical stress values in the gate region by 1.3–1.5 times depending on the specific power dissipated.

The degradation of GaN HFETs depends on the actual power supply modes, input power level, and class of operation of the amplifier. In this case, the thermal degradation effects that are amplified in class AB mode are more pronounced than the effects of strong fields in class E mode. Therefore, in order to determine the MTTF in practical microwave applications, GaN HFETs should be characterized under the conditions of actual supply voltages, microwave power, and the class of operation of the power amplifier.

A sharp decrease in MTTF and rapid (within a few hours) destruction occurs in contemporary GaN-heterotransistors at junction temperatures greater than 320–350°C.

While GaN HFETs have outperformed other semiconductors currently used in industry (such as GaAs, Si, InP, etc.) in terms of their technical and performance characteristics, it is necessary to take into account physical limitations in their design and fabrication to eliminate the possibility of degradation in operation due to the presence of the described degradation mechanisms, as well as to control the thermal and electrical modes of GaN HFETs in operation.

[4] www.wolfspeed.com. Accessed January 12, 2024.

[5] www.ums-rf.com. Accessed January 12, 2024.

[6] Final Report Summary – EUSIC (High Quality European GaN-Wafer on SiC Substrates for Space Applications). https://cordis.europa.eu/project/id/242360/reporting/pl.Accessed January 12, 2024.

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Translated from Russian into English by L. Bychkova
Edited for English language and spelling by Thomas A. Beavitt