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RESEARCH ARTICLE

Technical and economic analysis of servers as computing system modules of the warehouse scale computer class

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Abstract

Objectives. The work set out to technically and economically analyze servers as computing modules of computing systems of the warehouse scale computer (WSC) class.

Methods. The research was carried out using the methods of mathematical analysis and modeling.

Results. The article provides a technical and economic analysis of computing modules or servers. Servers are created on the basis of Xeon (Intel) class microprocessors and the like. An overview of the microprocessor subclasses is given along with an indication of server organization options, as well as their main components and primary areas of use. Server reliability is a complex property that may include durability, maintainability and persistence, or certain combinations of these properties depending on the purpose of the object and the conditions of its use. To ensure maximum reliability, backup elements, including arrays of disks and power supplies, as well as backup servers, are used alongside special solutions, including the use of hot swapping and connection, checking and correction of random access memory errors, and temperature control of server compartments.

Conclusions. The review of options for organizing servers and their main components allows permits the conclusion that their operation is sufficiently reliable. However, servers integrated into the WSC class have special requirements, namely, continuity of operation in 24/7 mode for long periods of time. This requires the development of methods for assessing the reliability of such highly reliable systems, including backup elements, in relation to hardware and software failures, as well as methods for predicting failures and measures to combat their consequences.

Keywords: reliability, backup elements, MP subclasses, error checking and correction, error correction, disk array, WSC class

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НАУЧНАЯ СТАТЬЯ

Технико-экономический анализ серверов как вычислительных модулей вычислительных систем класса WSC

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Резюме

Цели. Целью работы является технико-экономический анализ серверов как вычислительных модулей вычислительных систем (ВС) класса WSC (warehouse scale computer).

Методы. Основные результаты работы получены с использованием методов математического анализа и моделирования.

Результаты. Проведен технико-экономический анализ вычислительных модулей или серверов на базе микропроцессоров класса Xeon (Intel, США) и им подобных. Приведен обзор подклассов микропроцессоров с указанием основных областей их использования, а также вариантов организации серверов и их основных составляющих. Надежность – комплексное свойство, которое, в зависимости от назначения объекта и условий его применения, может включать безотказность, долговечность, ремонтопригодность и сохраняемость или определенные сочетания этих свойств. Для обеспечения максимальной надежности сервера используют как резервирующие элементы – массивы дисков и блоков питания, так и резервные серверы, и специальные решения: использование горячей замены и подключения, методы повышения надежности оперативной памяти Error Checking and Correction для коррекции ошибок модулей оперативной памяти, контроль температурных режимов отсеков сервера.

Выводы. Проведенный обзор вариантов организации серверов и их основных составляющих позволяет сделать вывод о достаточно высокой надежности их функционирования. От серверов, объединенных в ВС класса WSC, как от системы, требуется непрерывность функционирования в режиме 24/7 в течение длительного времени. Это требует разработки методик оценки надежности таких высоконадежных систем, включающих резервные элементы, по отношению к отказам аппаратуры и программного обеспечения, а также методик прогнозирования отказов и мер борьбы с их последствиями.

Ключевые слова: надежность, резервирующие элементы, подклассы микропроцессоров, error checking and correction , коррекция ошибок, массив дисков, класс WSC

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INTRODUCTION

A server has many characteristics such as reliability, performance, form factor, power consumption, etc., which are in turn made up of a set of properties of the individual nodes that make up the server [1].

Performance, which is primarily determined by the amount and speed of computation, also depends on the type of tasks performed. As the required amount of computation increases, the performance of components, especially the processor, should also be increased.

Significant reductions in power consumption, as well as improved power efficiency and infrastructure flexibility, can be achieved using the modular design principles of blade server architecture [2].

Server power consumption is primarily affected by its available resources, such as the number of processors (and cores), their clock speeds, the amount of random access memory (RAM), the performance and capacity of the storage subsystem, as well as the performance of the network interfaces.

Depending on the task, the choice of hardware selection can include increases in available resources for improved performance or their decrease as a means of saving energy. Up to a certain point, resources may be increased by increasing memory capacity and performance, as well as the number of processors. However, after reaching this limit, further performance increases by such means becomes inefficient and uneconomical. In such cases, resources may be increased by other methods, for example, by parallelizing tasks between several servers or application optimization. Reductions in server resources are usually aimed at reducing the size and power consumption of installations [3].

PROCESSOR

Processor key characteristics [4] include performance, power consumption, and energy efficiency (the average amount of energy consumed per instruction executed).

Processor performance is defined as the execution speed of program code instructions, i.e., the number of instructions processed per unit time (instructions per second, IPS). This can be expressed mathematically as follows:

$$\text{Perfomance} = \frac{\text{Number of instructions}}{\text{Time of execution}} = \text{IPS}. \quad (1)$$

Instead of the number of instructions per time unit, it is more convenient to consider the number of program code instructions executed per processor clock (instructions per cycle, IPC).

$$\text{Perfomance} = \frac{\text{Number of instructions}}{\text{Number of clocks}} \times \times \frac{\text{Number of clocks}}{\text{Execution time}} = \text{IPC}. \quad (2)$$

Processor performance is directly related to both the clock frequency F and the number of instructions executed per IPC clock.

Thus, there are two main approaches to improving processor performance [5]: the first is to increase the clock frequency, while the second is to increase the number of instructions executed per clock. In practice, both approaches are usually applied simultaneously, since clock frequency parameters and the number of instructions executed per clock are interrelated.

The dependence of processor power consumption on its clock frequency appears as follows:

$$\text{Power} = CU^2F, \quad (3)$$

where C is the dynamic capacitance of the processor; U is the processor supply voltage; F is the processor operating frequency.

In other words, the power consumed by the processor is proportional to the clock frequency, the square of the processor's supply voltage and its dynamic capacitance. Since the clock frequency is directly related to the supply voltage, the power consumption varies nonlinearly with the processor frequency. Consequently, processor performance and power consumption are also related in a nonlinear manner.

Increasing the clock frequency gives only a marginal increase in performance and is accompanied by a much larger increase in processor power consumption [6].

Currently, the focus in improving processor performance has shifted from increasing clock frequency to achieving high performance levels with minimal energy consumption. The key indicator [7] in this context is the processor energy efficiency (energy per instruction, EPI), which is measured as the average amount of energy consumed per executed instruction:

$$\text{EPI} = \frac{\text{Power (J)}}{\text{Number of instructions}}. \quad (4)$$

Processor performance per 1 watt of power consumed will be as follows:

$$\frac{\text{Perfomance}}{\text{Power}} = \frac{\left(\frac{\text{Number of instructions}}{\text{Time}}\right)}{\left(\frac{\text{Power}}{\text{Time}}\right)} = = \frac{\text{Number of instructions}}{\text{Power}} = \frac{1}{\text{EPI}}. \quad (5)$$

Consequently:

$$EPI = \frac{Power}{Perfomance}. \quad (6)$$

One of the approaches to creating a power-efficient processor is to use multicore architecture [8]. This increases performance by increasing the number of instructions executed per clock without increasing and sometimes even decreasing the clock frequency. Theoretically, when increasing the number of cores from 1 to 2, it is possible to maintain the same performance by reducing the clock frequency of each core by a factor of 2.

The performance gain in this case can be estimated as a reduction of the program execution time when using a multicore processor *tn* compared to its execution time on a single-core processor *t*1. Thus, the performance gain will be equal to [9]:

$$\frac{t1}{tn} = 1 - p\left(1 - \frac{1}{n}\right), \quad (7)$$

where p is the share of program code instructions that can be executed in parallel; n is the number of the processors.

The graphical dependence of performance gain on the number of processor cores is shown in Fig. 1.

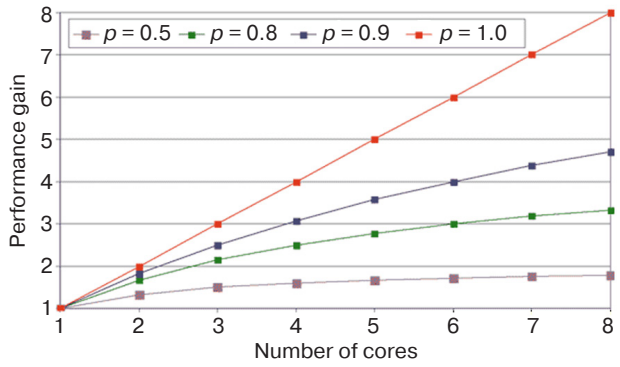

Fig. 1. Dependence of performance gain on the number of processor cores

Multicore architecture significantly improves performance, especially when running multiple applications simultaneously. Under perfect conditions, each application can run on a separate processor core.

Intel Xeon microprocessors

Intel Xeon class microprocessors (Intel, USA) [10] are built on the same microarchitectures as desktop processors (x86), but with the addition of server-specific features.

The design and implementation of server processors is characterized by considerable complexity as compared to desktop systems due to the required implementation of many specific features. Due to the increasing complexity and development time of new architectures using the 10-nm process technology, process technologies used with different processor families such as Xeon, Opteron (AMD, USA) and Baikal-T1 (Baikal Electronics, Russia) are tending to converge.

Crystalwell technology can help to overcome the limitations of low system memory bandwidth and demonstrate improved results in HD video processing and math operations. With Broadwell processors, 4368 HD video streams can be executed simultaneously, representing a 40% increase over the 3120 streams on their Haswell processors.

Intel Xeon E3 v6 processors are available in 8 models, none of which offer reduced power consumption. In this lineup, the use of embedded dynamic random access memory (DRAM) has also been abandoned. However, as before, processors with index 1xx5 v6 are equipped with their own graphics cores.

The main changes include the transition to the Kaby Lake architecture while retaining the 14-nm process technology. In addition, the maximum memory bandwidth has been increased to 37.5 GB/s and frequencies have been increased to DDR4-2400 and DDR3L-1866.

The performance gain when switching from E3 to E5 processors and using two E5 processors is shown in Fig. 2.

Intel tests show the following result: performance increases 1.5 times when switching from E3 to E5 processors and another 2 times when doubling the number of processors. Switching to a 4-processor system provides similar linear performance gains. Performance improves similarly with new processor generations, for example, when switching from E3 v5 or v6 to E5 v4.

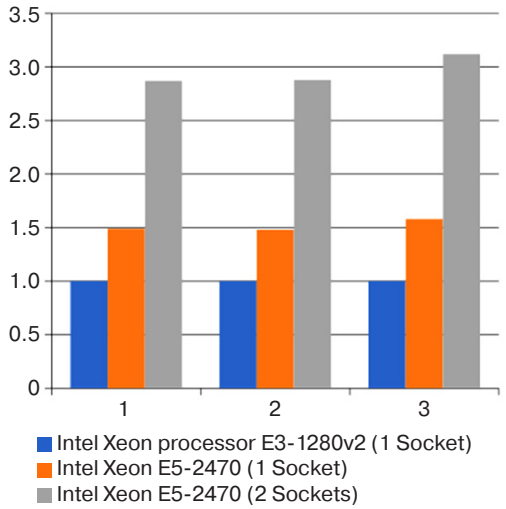

Fig. 2. Change in performance when switching from E3 to E5: (1) SPECint_ratebase 2006, (2) SPECfp*ratebase 2006, (3) SPECjbb*2005

In the future, Broadwell-EX processors will be replaced by Skylake Purley. These new processors will feature 6-channel DDR4 RAM controllers (instead of the current generation's 4-channel), AVX-512 instruction set, Omni-Path bus, Cannonlake graphics support, and embedded field-programmable gate arrays (FPGAs). Embedded FPGAs enable the processor configuration to be optimized for specific tasks, which configuration is not available in the Skylake architecture.

Intel Xeon D processors

Intel Xeon D processors [11] are the successors to the Atom line, but are designed for lightweight server solutions. These processors are systems-on-a-chip and include x86 computing cores, 10G network card, I/O ports (including PCIe[1]), DDR4 controller and SATA interfaces. They are manufactured using a 14nm process technology.

Intel Xeon D-15xx, whose main application area is networking, cloud storage and enterprise storage systems, offer new opportunities to optimize diverse workloads and infrastructures.

AMD Opteron server processors

Server processors from AMD are represented by five series: Opteron 3000, 4000, and 6000, A-series based on ARM-architecture, as well as hybrid processors X-series [12]. These processors, which are primarily designed for web hosting, are characterized by their affordable price. They support DDR3-1866 MHz memory.

Generally, the Opteron line of processors combine good performance, a large number of cores, and a competitive price. Rather than using hyperthreading technology analogs, the performance of Opteron processors is increased by adding more physical cores.

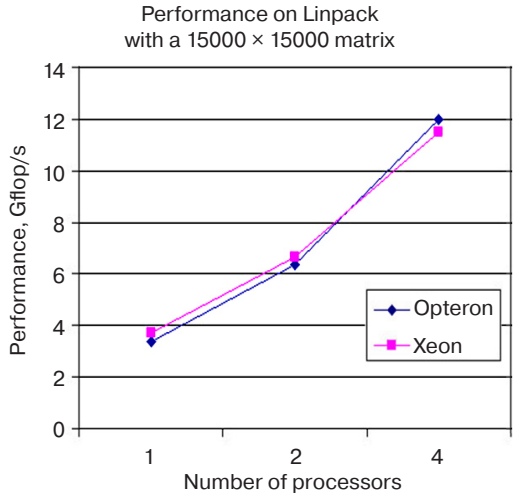

Fig. 3. Performance comparison of Intel Xeon and AMD Opteron processors

Based on the X2150 processor, the X2170 hybrid processor is a fully integrated x86 architecture unit that includes a CPU, graphics processor and I/O controller. It features low power consumption to reduce the total cost of ownership of data centers and adapt to the requirements of high-performance server platforms.

The main tasks for which these server processors are designed include organizing delivery and distribution networks, video preprocessing, console desktop clients, rendering, transcoding, and video streaming.

Combining CPU and GPU technologies in an ultra-dense form factor can result in large performance-per-watt gains over traditional solutions.

Baikal-T1 processor

The Baikal-T1 processor [13], which is based on 2 computing cores having a clock frequency of 1.2 GHz, is implemented on a 28-nm process belonging to the MIPS Warrior P5600 r5 family of Imagination Technologies (United Kingdom). It uses the MIPS32 architecture with support for the extraordinary instruction execution paradigm and the ability to combine up to 6 cores into a single cluster. The P5600 r5 cores support OmniShield hardware zonal data protection technology and 128-bit SIMD-commands[2] for high-speed parallel processing, especially in multimedia applications.

The processor is equipped with 1 MB of high-performance coherent cache memory and an integrated RAM controller with DDR3-1600 support. It includes integrated interfaces: 1 × 10 Gbit Ethernet, 2 × 1 Gbit Ethernet, PCIe Gen.3 x4, SATA 3.0, and USB 2.0. Due to the processor's low power consumption at less than 5 watts, it may be used to develop quiet systems that do not require active cooling.

The main anticipated applications for this processor are industrial automation, embedded systems, and communications.

RANDOM ACCESS MEMORY

Server memory differs from desktop memory due to its inclusion of parity and error correction code (ECC) modules. This type of memory includes additional functionality to provide greater stability, such as the use of register buffered memory. Thus, server memory is manufactured according to different standards than desktop systems.

A key characteristic of server RAM is fault tolerance. Many servers are designed to run mission-critical applications that place high demands on memory. The level of fault tolerance is provided both through

[1] Peripheral component interconnect express is a computer bus that provides point-to-point connectivity using a high-performance serial communications protocol.

[2] Single instruction, multiple data—a principle of computer computing that enables parallelism at the data level.

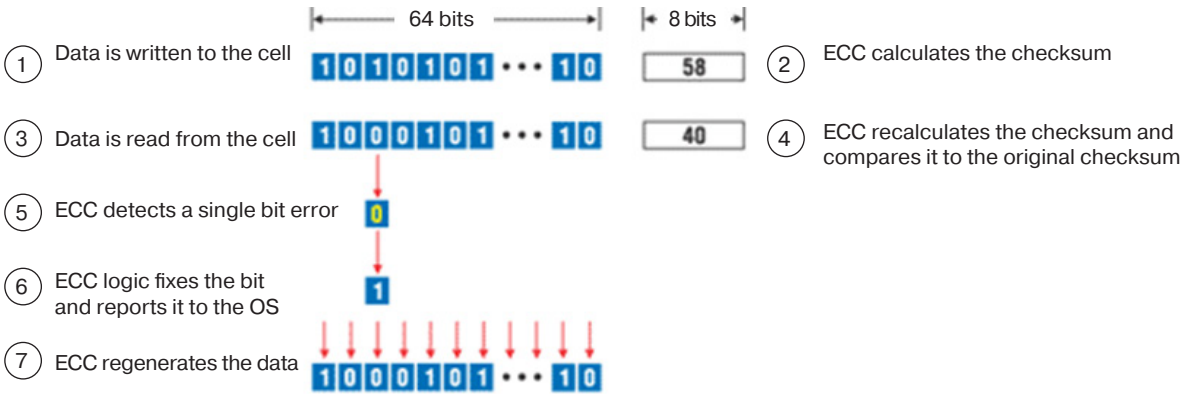

Fig. 4. Single-bit error detection and correction diagram. OS—operating system

improvements in the chip manufacturing process and through the use of memory error protection technologies such as ECC [14].

There are two main ways to protect against memory errors:

1. Module testing, i.e., regular checking of memory status to detect and correct problems.
2. Use of error detection and correction technologies, i.e., the introduction of technologies for automatically detecting and correcting memory errors.

ECC technology, which significantly reduces the probability of memory errors, provides single-bit error detection and correction, along with multibit error detection. This is an important feature for server RAM where reliability and error tolerance are critical. The corresponding operational mechanism is demonstrated in Fig. 4.

Memory errors can also cause significant downtime in database server applications. If an error occurs, database recovery can take several hours due to the need to recover data from transaction log entries that have not yet been entered into the database.

Advanced ECC technology, which is designed to correct multibit errors on a single DRAM chip, significantly increases system reliability by supporting data recovery even in case of failure of the entire chip.

Since four bits from each chip are distributed to four ECC devices (one bit for each ECC device), an error in one chip can correct up to four single-bit errors (Fig. 5).

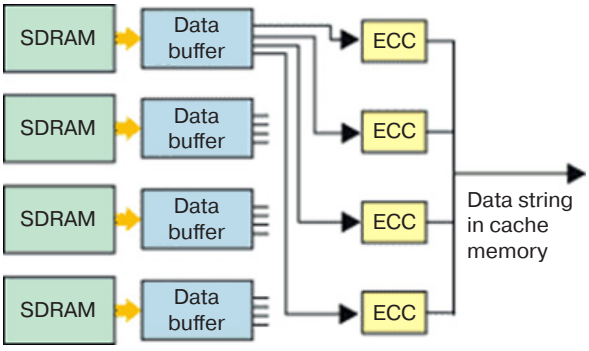

Fig. 5. Advanced ECC operation diagram

The Chipkill mechanism is used to deal with multibit errors on individual chips, including failure of all data bits. This mechanism provides higher protection and reliability compared to traditional methods.

DDR4 DRAM is currently the most advanced and widely used RAM technology. However, DDR5 DRAM is already under development. DDR5 is expected to provide twice the capacity of DDR4 modules, as well as increased bandwidth. DDR5 memory, which is to be manufactured using a 10-nm process, will initially be available in capacities ranging from 1 GB to 4 GB.

STORAGE SUBSYSTEM

An important aspect is availability of drives: server drives must remain functional and active at all times, while desktop PC drives can be placed in standby mode when access is not required [15].

For reliability and performance, redundant arrays of independent disks are often used to combine multiple disk drives for increased fault tolerance and performance. Important factors that influence drive selection include the connection interface, capacity, and drive structure. Here, the expected data to be stored, as well as its importance and the requirements of the installed applications, also play a significant role.

Hard disk drives (HDD), which represent the classic storage solution, provide an acceptable level of reliability; their performance depends on factors such as rotation speed, interface and cache size. HDDs range from 7200 to 15000 rpm depending on performance requirements. However, higher rotational speeds result in higher power consumption and higher cooling requirements. An additional potential problem consists in vibration due to the varying speeds of the disks, which can be disruptive if the disks are in different write cycles. To prevent such problems, it is recommended to use disks with the same rotation speed within the same server. It is also worth noting that the service life of hard disks is limited by their mechanical wear and tear.

Solid state drives (SSDs) have no moving parts, eliminating mechanical wear and vibration. They use flash memory to store data, allowing them to achieve I/O performance that can be hundreds of times faster than HDDs. SSDs, which do not require power for the electric motor, consume about one-fifth of the power of HDDs.

When selecting a drive, it is important to keep in mind that SSDs have a limited data retention period when turned off. If the SSD is used for backup storage, the information will be available for a maximum of 10 years. However, this period may be shortened due to heavy use and exposure to ambient temperatures.

A promising direction in the development of data storage systems is the transition to non-volatile memory of the NAND[3] type. Such memory eliminates the main causes of delays in the data exchange channel between the system and the solid-state drive. Using the PCIe bus directly, without additional adapters (SATA, SAS, etc.), reduces latency at the controller level. Selecting NVMe[4] helps to eliminate latency at the software level (both in the controller firmware and system drivers) as well as significantly increasing the level of parallelism when exchanging data streams over the bus.

The NVMe interface is a key benefit for server applications, especially when processing large numbers of requests simultaneously. Switching to NVMe can significantly improve disk array efficiency by scaling the number of queues and commands.

The evolution of storage systems continues with the development of new storage technologies, such as pulse code modulation and other promising solutions, which may lead to significant improvements in access speed and overall performance in the future.

Crossbar estimates that resistive random-access memory (RRAM) modules will deliver write speeds 20 times faster than NAND flash memory, reaching 140 MB/s compared to NAND's 7 MB/s. Read speeds for RRAM will be around 17 MB/s. An additional advantage of RRAM is the longevity of data storage, which can be up to 20 years, as compared to only 1–3 years for NAND.

Magnetoresistive random-access memory is also being considered as an alternative to NAND flash memory. It stands out for its high data access speed and reliability under unfavorable environmental conditions. Magnetoresistive memory can operate at very high temperatures, making it particularly suitable for extreme environments such as military and space applications.

CONCLUSIONS

The review of server organization options and their main components allows us to conclude the sufficient reliability of their operation. However, servers combined in the WSC class as a system additionally require continuous operation in 24/7 mode for long periods of time. This, in turn, requires the development of methods for assessing the reliability of such highly reliable systems, including redundant elements to compensate for hardware and software failures, as well as methods for predicting failures and measures to combat their consequences.

Authors' contribution
All authors equally contributed to the research work.

[3] Not AND is a universal two-input logic element, Schaeffer stroke.

[4] NVM Express is non-volatile memory host controller interface specification—access interface to solid state drives connected via PCI Express bus.

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