Information systems. Computer sciences. Issues of information security

Информационные системы. Информатика. Проблемы информационной безопасности

UDC 681.3
https://doi.org/10.32362/2500-316X-2024-12-6-20-25
EDN PWDKPB

RESEARCH ARTICLE

Analysis and selection of the structure of a multiprocessor computing system according to the performance criterion

Grigory V. Petushkov @,
Alexander S. Sigov

MIREA – Russian Technological University, Moscow, 119454 Russia
@ Corresponding author, e-mail: petushkov@mirea.ru

Abstract
Objectives. Analysis of the various architectures of computing systems (CSs) used in recent decades has allowed us to identify the most common structures. One of the key features is the use of mass-produced equipment to create data processing subsystems (for example, multicore processors and high-capacity semiconductor memory), as well as network equipment to build communication subsystems. This reduces hardware costs and allows typical or cluster configurations to be created, which is especially important for expensive CSs. The desire to achieve high computational speed and performance in such CSs requires minimizing the time to complete the task and balancing time delays both in data processing subsystems and in the communication subsystem which provides data transmission inside the CS. The aim of this work is to analyze computing modules (CMs) and structures on the basis of which the construction of cluster CSs is carried out.
Methods. The main results of the work were obtained using methods of mathematical analysis and modeling.
Results. The study considers the structure of modern multicore microprocessors as the basis for building CMs of cluster CSs. As the number of cores in the microprocessor structure increases, the communication network which unites them into a single structure becomes more complicated. It has been shown that in new developments of microprocessors, communication between cores is performed in the form of a network. The microprocessors themselves are MIMD structures in accordance with the well-known Flynn classification.
Conclusions. The proposed method of selecting an effective structure of a CS allows us to obtain the optimal structure of a CS according to the criterion of performance.

Keywords: InfiniBand network, performance, microprocessors, computing modules, Halstead metrics, analysis

• **Submitted:** 18.10.2024 • **Revised:** 26.10.2024 • **Accepted:** 05.11.2024

For citation: Petushkov G.V., Sigov A.S. Analysis and selection of the structure of a multiprocessor computing system according to the performance criterion. *Russ. Technol. J.* 2024;12(6):20–25. https://doi.org/10.32362/2500-316X-2024-12-6-20-25

Financial disclosure: The authors have no financial or proprietary interest in any material or method mentioned.

The authors declare no conflicts of interest.

НАУЧНАЯ СТАТЬЯ

Анализ и выбор структуры многопроцессорной вычислительной системы по критерию быстродействия

Г.В. Петушков @,
А.С. Сигов

МИРЭА – Российский технологический университет, Москва, 119454 Россия
@ *Автор для переписки, e-mail: petushkov@mirea.ru*

Резюме

Цели. Анализ различных архитектур вычислительных систем (ВС), использовавшихся в последние десятилетия, позволил выделить наиболее распространенные структуры. Одной из ключевых особенностей является использование серийно производимого оборудования для создания подсистем обработки данных (например, многоядерные процессоры и полупроводниковая память большой емкости) и сетевого оборудования для построения коммуникационных подсистем. Это снижает затраты на оборудование и позволяет создавать типовые или кластерные конфигурации, что особенно важно для дорогостоящих ВС. Стремление достичь высокой вычислительной скорости и производительности в таких ВС требует минимизации времени на выполнение задачи и балансировки временных задержек как в подсистемах обработки данных, так и в коммуникационной подсистеме, обеспечивающей передачу данных внутри ВС. Целью работы является анализ вычислительных модулей (ВМ) и структур, на основе которых проводится построение кластерных ВС.

Методы. Основные результаты работы получены с использованием методов математического анализа и моделирования.

Результаты. Рассмотрена структура современных многоядерных микропроцессоров (МП), являющихся основой построения ВМ кластерных ВС. По мере увеличения числа ядер в структуре МП усложняется коммуникационная сеть, объединяющая их в единую структуру. Показано, что в новых разработках МП коммуникация между ядрами выполняется в виде сети, а сами МП представляют собой MIMD-структуры (множественный поток команд, множественный поток данных) в соответствии с известной классификацией Флинна.

Выводы. Предложенная методика выбора эффективной структуры ВС позволяет получить оптимальную структуру ВС по критерию быстродействия.

Ключевые слова: сеть InfiniBand, быстродействие, микропроцессоры, вычислительные модули, метрики Холстеда, анализ

• **Поступила:** 18.10.2024 • **Доработана:** 26.10.2024 • **Принята к опубликованию:** 05.11.2024

Для цитирования: Петушков Г.В., Сигов А.С. Анализ и выбор структуры многопроцессорной вычислительной системы по критерию быстродействия. *Russ. Technol. J.* 2024;12(6):20–25. https://doi.org/10.32362/2500-316X-2024-12-6-20-25

Прозрачность финансовой деятельности: Авторы не имеют финансовой заинтересованности в представленных материалах или методах.

Авторы заявляют об отсутствии конфликта интересов.

INTRODUCTION

Modern multicore microprocessors form the basis for constructing computing modules (CMs) of cluster computing systems (CSs). Along with an increase in the number of cores in the microprocessor structure, the communication network which unites them into a single structure becomes more complex. In improved microprocessor designs, communication between cores is performed in the form of a network. The microprocessors themselves are multiple instruction and multiple data (MIMD) structures in accordance with the well-known Flynn classification [1–3].

At the next level, one or more microprocessors are used as the basis for a CM of a CS cluster cell. In a CM, microprocessors are combined with RAM modules by standard peripheral component interconnect (PCI) class, i.e., Express 3.0 class interfaces. They can also be combined with a switch that provides communication between all microprocessors and all memory modules [4].

At the system level, a relatively large number of CMs in the clustered systems are interconnected by networking facilities. As a rule, this requires several networks, such as [5]:

- a network providing data transfer between CMs in the process of task solving;
- a network that connects individual CMs to a data warehouse used both for initial task data loading and for storing results;
- a service network associated with the control of CS, through which the information on monitoring the performance of the CM and entire CS is circulated.

The fastest of these networks should be the former network, also referred to as a data transfer network and executed as an InfiniBand network (IBA) [6]. This network supports the densest data transfer traffic during the process of task solving in CS. As the number of CM in the CS increases, the processing time for a task decreases due to the increase in the number of processing devices, and the "time overhead" of data transfer between CM will increase [7].

The question then arises about the optimal number of CMs in the CS, providing the minimum time of task execution at known characteristics of CMs and data transmission network. This task is formulated in the work as a cluster CS structure selection problem [8].

METHODOLOGY FOR SELECTING AN EFFICIENT STRUCTURE OF THE ALL-ROUND SYSTEM, OPTIMAL BY THE CRITERION OF FAST PERFORMANCE

Let us evaluate the performance of the CSs using the IBA network when the number of microprocessors and CMs increases [9]. The performance growth of such systems with an increase in the number of CMs is nonlinear. This is because the increase in the number of CMs leads to an increase in the "overhead" associated with the time required for data exchange between modules. The time spent on data exchange especially increases when CMs interact through the network, where delays occur and traffic volume increases.

In order to analyze the influence of these "overheads" [10], let us consider an idealized case of executing a well-parallelized program which consists of N parallel fragments distributed over K CMs, where $N > K$.

The program execution time in the considered case can be estimated as follows:

$$T_{\text{pr}} = T_{\text{calc}} + T_{\text{exch}}, \qquad (1)$$

wherein T_{calc} is the time spent on calculations in CMs; T_{exch} is the time spent on data exchange between CMs.

T_{calc} value can be estimated taking into account the capacity of one CM P_{CM} and their number K by the formula:

$$T_{\text{calc}} = \frac{G}{KP_{\text{CM}}}, \qquad (2)$$

wherein G is an estimate of the number of operations in the program.

G value can be obtained by analyzing the program algorithm using, for example, Halstead metrics.

The time consumption for exchanging a data packet T_{p} in a data network is defined as follows:

$$T_{\text{p}} = T_{\text{n}} + T_{\text{d}} + \frac{Q}{V}, \qquad (3)$$

wherein T_{n} is the delay of data packet formation in the network adapter; T_{d} is the delay of packet transmission in the network, associated with delays in the switch; Q is the amount of transmitted data in the data packet; V is the velocity of data transmission in the network.

Let us consider the data transmission network as part of the CS [11], since the volume of traffic therein is much larger than that in the service network. Analyzing the time of data exchange as an "overhead" in the process of computation, in the first approximation T_{exch} can be estimated taking the limited network bandwidth into account as follows:

$$T_{\text{exch}} = K\frac{Q}{V}. \qquad (4)$$

Let us explain the derivation of Eq. (4) in greater detail on the example of a system consisting of K CMs. Since the amount of traffic of each CM is proportional to the number of CMs, let us assume that each CM forwards packets to other CMs after completing the execution of its program fragment. The total communication time can be estimated by combining the traffic of all CMs [12] forwarded over the network. This time is shown in the form (4).

The amount of data in bytes of the exchange packet is related to the number of operations in the executed program G (computational complexity of the algorithm) as follows:

$$Q = CGL, \tag{5}$$

wherein C is the coefficient characterizing the class of algorithms being executed with respect to data connectivity (algorithms with higher data connectivity are characterized by a higher intensity of exchanges between CMs and a higher value of the coefficient C), and L is the share of computational operations in the executed program fragment ($L \approx 1$).

Taking Eqs. (2)–(5) into account, Eq. (1) can be rewritten as:

$$T_{\text{pr}} = \frac{G}{KP_{\text{CM}}} + \frac{CGL}{V}K. \tag{6}$$

It follows from the above expression (6) that an increase in K leads to a decrease in the time spent on computation and an increase in the time duration for data exchange in the CS. Thus, the characteristics of the data transmission network will strongly affect the CS performance.

Equation (6) can be used to determine the optimal value of the number of CMs K_{opt}, providing the minimum value of the program execution time T_{pr}. The value of the coefficient k, determining the number of CMs in the full CS, is calculated based on the condition $dT_{\text{pr}}/dk = 0$ as follows:

$$K_{\text{opt}} = \sqrt{\frac{V}{CP_{\text{CM}}L}}. \tag{7}$$

For modern CSs [13], the coefficient values are at the level of unity for network throughput V = 10 Gbytes/s and data processing speed of 10 billion operations per second. However, for the coefficient values C = 0.01 bytes/operation, characterizing algorithms with weak data connectivity, it can reach 10.

Along with an increase in the data network bandwidth, the number of CMs in the system can be increased without significant performance degradation due to the time spent on data exchange. Using an optical bus with a data transfer rate of V = 1, Tbyte/s for the data network can increase the optimal number of CMs by more than 10 times (up to 100 CMs), significantly improving the efficiency of multiprocessor and multi-module CS.

Equation (7) for the coefficient will be referred to as the rule of "selecting the effective structure of the CS" and we note its important practical significance in CS design. The methodology of structure selection for a cluster CS includes several stages [14, 15]:

1. CM performance analysis.
2. Estimation of the data transfer rate in the fastest CS data network.
3. Analysis of the algorithm for determining the data cohesion coefficient C.
4. Determination of the coefficient according to Eq. (7).

In actual CS, the number of CMs, as a rule, exceeds the value of 10. This is due to the development of efficient CS designs. However, with the growth of data transmission speeds in the network, the calculated and actual numbers of CMs will be better coordinated.

CONCLUSIONS

1. The most efficient ratio structures of cluster CSs in terms of "cost/performance" are built on the basis of standard equipment of IBA and Ethernet networks.
2. A methodology for selecting an effective structure of the CS is proposed on the basis of the analysis of time costs for data processing and transmission in the CS. This allows the optimal structure of the CS to be obtained according to the criterion of speed. The methodology includes the following steps:

- analysis of the specifics of data exchange between CMs depending on the algorithm of the task solving;
- analysis of CM performance depending on the equipment used;
- analysis of the bandwidth capacity of the data transmission network in CS;
- selection of the CS structure as a choice of the optimal number of CMs in accordance with Eq. (7).

Authors' contribution

All authors equally contributed to the research work.

REFERENCES

1. Voevodin V.V., Voevodin Vl.V. *Parallel'nye vychisleniya* (*Parallel Computing*). St. Petersburg: BHV-Petersburg; 2002. 608 p. (in Russ.).
2. Orlov S.A., Tsil'ker B.Ya. *Organizatsiya EVM i system* (*Organization of Computers and Systems*). St. Petersburg: Piter; 2016. 688 p. (in Russ.).
3. Henessey J.L., Patterson D.A. *Komp'yuternaya arkhitektura. Kolichestvennyi podkhod* (*Computer Architecture. A Quantitative Approach)*: transl. from Engl. 5th ed. Moscow: Tekhnosfera; 2016. 936 p. (in Russ.).
[Henessey J.L., Patterson D.A. *Computer Architecture. A Quantitative Approach.* 5th ed. Morgan Kaufmann; 2011. 856 p.]
4. Kirk B., Sharad S., Stanley V. How to succeed in an economy of abundance of memory? *Otkrytye sistemy = Open Systems. DBMS*. 2016;2:25–32 (in Russ.).
5. Sugak E.V. *Prikladnaya teoriya nadezhnosti. Praktikum* (*Applied Reliability Theory. The Workshop. Textbook*). Moscow: Lan; 2023. 312 p. (in Russ.). ISBN 978-5-507-47014-3
6. Kovalenko S.M. Evaluation of the reliability of information management systems based on continuous models. *Voprosy radioelektroniki = Questions of Radio Electronics*. 2005;4(2):143–146 (in Russ.).
7. Polovko A.M., Gurov S.V. *Osnovy teorii nadezhnosti* (*Fundamentals of Reliability Theory)*. St. Petersburg: BHV-Petersburg; 2006. 702 p. (in Russ.). ISBN 5-94157-541-6
8. Cherkesov G.N. *Nadezhnost' apparatno-programmnykh kompleksov* (*Reliability of Hardware and Software Complexes*). St. Petersburg: Piter; 2005. 479 p. (in Russ.). ISBN 5-469-00102-4
9. Kovalenko S.M., Platonova O.V. Analysis of the operational efficiency of complex automation systems and the calculation of their reliability on the basis of continuous models. *Izvestiya vysshikh uchebnykh zavedenii. Mashinostroenie = BMSTU J. Mechanical Engineering.* 2014;8(653):75–89 (in Russ.). http://doi.org/10.18698/0536-1044-2014-8-75-79
10. Podgorny Y.V., Antonovich A.N., Petrushin A.A., Sigov A.S., Vorotilov K.A. Effect of metal electrodes on the steady-state leakage current in PZT thin film capacitors. *J. Electroceram.* 2022;49:15–21. https://doi.org/10.1007/s10832-022-00288-5
11. Abdullaev D.A., Milovanov R.A., Volkov R.L., Borgardt N.I., Lantsev A.N., Vorotilov K.A., Sigov A.S. Ferroelectric memory: state-of-the-art manufacturing and research. *Russ. Technol. J*. 2020;8(5):44–67 (in Russ.). https://doi.org/10.32362/2500-316X-2020-8-5-44-67
12. Konyukhova O.V., Kravtsova E.A., Lukyanov P.V. *Tekhnicheskoe i programmnoe obespechenie vychislitel'nykh mashin i system* (*Technical and Software Support of Computers and Systems*). Infra-Inzheneriya; 2023. 200 p. (in Russ.). ISBN 978-5-9729-1186-8
13. Zhuravlev A.A. *Organizatsiya i arkhitektura EVM. Vychislitel'nye sistemy* (*Organization and Architecture of Computers. Computer Systems*). Lan; 2022. 144 p. (in Russ.). ISBN 978-5-507-48089-0
14. Gelbukh C.A. *Seti EVM i telekommunikatsii. Arkhitektura i organizatsiya* (*Computer Networks and Telecommunications. Architecture and Organization*). Lan; 2019. 208 p. (in Russ.). ISBN 978-5-8114-3474-9
15. Andreev A.M., Mozharov G.P., Syuzev V.V. *Mnogoprotsessornye vychislitel'nye sistemy. Teoreticheskii analiz, matematicheskie modeli i primenenie* (*Multiprocessor Computing Systems. Theoretical Analysis, Mathematical Models and Applications*). Moscow: Bauman Press; 2011. 336 p. (in Russ.). ISBN 978-5-7038-3439-6

СПИСОК ЛИТЕРАТУРЫ

1. Воеводин В.В., Воеводин Вл.В. *Параллельные вычисления*. СПб.: БХВ-Петербург; 2002. 608 с.
2. Орлов С.А., Цилькер Б.Я. *Организация ЭВМ и систем*. СПб.: Питер; 2016. 688 с.
3. Хенесси Д.Л., Паттерсон Д.А. *Компьютерная архитектура. Количественный подход*. 5-е изд. М.: Техносфера; 2016. 936 с.
4. Кирк Б., Шарад С., Стенли В. Как преуспеть в условиях экономики изобилия памяти? *Открытые системы. СУБД*. 2016;2:25–32.
5. Сугак Е.В. *Прикладная теория надежности. Практикум.* М.: Лань; 2023. 312 с. ISBN 978-5-507-47014-3
6. Коваленко С.М. Оценка надежности информационно-управляющих систем на основе непрерывных моделей. *Вопросы радиоэлектроники.* 2005;4(2):143–146.
7. Половко А.М., Гуров С.В. *Основы теории надежности*. СПб.: БХВ-Петербург; 2006. 702 с. ISBN 5-94157-541-6
8. Черкесов Г.Н. *Надежность аппаратно-программных комплексов*. СПб.: Питер; 2005. 479 с. ISBN 5-469-00102-4
9. Коваленко С.М., Платонова О.В. Анализ задачи эффективной эксплуатации комплексов систем автоматизации и расчеты надежности на основе непрерывных моделей. *Известия вузов. Машиностроение*. 2014;8(653):75–89. http://doi.org/10.18698/0536-1044-2014-8-75-79
10. Podgorny Y.V., Antonovich A.N., Petrushin A.A., Sigov A.S., Vorotilov K.A. Effect of metal electrodes on the steady-state leakage current in PZT thin film capacitors. *J. Electroceram.* 2022;49:15–21. https://doi.org/10.1007/s10832-022-00288-5
11. Абдуллаев Д.А., Милованов Р.А., Волков Р.Л., Боргардт Н.И., Ланцев А.Н., Воротилов К.А., Сигов А.С. Сегнетоэлектрическая память: современное производство и исследования. *Russian Technological Journal*. 2020;8(5):44–67. https://doi.org/10.32362/2500-316X-2020-8-5-44-67
12. Конюхова О.В., Кравцова Э.А., Лукьянов П.В. *Техническое и программное обеспечение вычислительных машин и систем.* Инфра-Инженерия; 2023. 200 с. ISBN 978-5-9729-1186-8

13. Журавлев А.А. *Организация и архитектура ЭВМ. Вычислительные системы*. Лань; 2022. 144 с. ISBN 978-5-507-48089-0
14. Гельбух С.А. *Сети ЭВМ и телекоммуникации. Архитектура и организация*. Лань; 2019. 208 с. ISBN 978-5-8114-3474-9
15. Андреев А.М., Можаров Г.П., Сюзев В.В. *Многопроцессорные вычислительные системы. Теоретический анализ, математические модели и применение*. Издательство МГТУ им. Н.Э. Баумана; 2011. 336 с. ISBN 978-5-7038-3439-6

About the authors

Grigory V. Petushkov, Vice-Rector, MIREA – Russian Technological University (78, Vernadskogo pr., Moscow, 119454 Russia). E-mail: petushkov@mirea.ru. https://orcid.org/0009-0006-0801-429X

Alexander S. Sigov, Academician at the Russian Academy of Sciences, Dr. Sci. (Phys.–Math.), Professor, President, MIREA – Russian Technological University (78, Vernadskogo pr., Moscow, 119454 Russia). E-mail: sigov@mirea.ru. Scopus Author ID 35557510600, ResearcherID L-4103-2017, RSCI SPIN-code 2869-5663, https://www.researchgate.net/profile/A_Sigov

Об авторах

Петушков Григорий Валерьевич, проректор, ФГБОУ ВО «МИРЭА – Российский технологический университет» (119454, Россия, Москва, пр-т Вернадского, д. 78). E-mail: petushkov@mirea.ru. https://orcid.org/0009-0006-0801-429X

Сигов Александр Сергеевич, академик Российской академии наук, д.ф.-м.н., профессор, президент ФГБОУ ВО «МИРЭА – Российский технологический университет» (119454, Россия, Москва, пр-т Вернадского, д. 78). E-mail: sigov@mirea.ru. Scopus Author ID 35557510600, ResearcherID L-4103-2017, SPIN-код РИНЦ 2869-5663, https://www.researchgate.net/profile/A_Sigov

Translated from Russian into English by Lyudmila O. Bychkova
Edited for English language and spelling by Dr. David Mossop